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Transmittal

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(Susanne C. Pelose)

Docket No.: 967_038
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Toshinobu Nakao et al.

Application No.: 10/722,752 Confirmation No.: 7293

Filed: November 26, 2003 Art Unit: 2138

For: SCAN TEST CONTROL METHOD AND SCAN TEST CIRCUIT Examiner: John P. Trimmings

CLAIM FOR PRIORITY AND SUBMISSION OF DOCUMENTS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In further response to the Office Action, dated April 3, 2006, Applicants hereby claim priority under 35 U.S.C. §119 based on the following prior foreign application filed in the following foreign country on the date indicated:

Japan	2003-067170	March 12, 2003

In support of this claim, a certified English language copy of the said original foreign application is filed herewith.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 50-0289, under Order No. 967_038 from which the undersigned is authorized to draw.

Dated: July 12, 2006

Respectfully submitted,

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Declaration

I, Shin Tanimura, a member of Hayase & Co. patent attorneys of 4F, The Sumitomo Building No.2, 4-7-28, Kitahama, Chuo-ku, Osaka-shi, Osaka 541-0041 Japan, hereby declare that I am the translator of the attached document and certify that the following is a true translation to the best of my knowledge and belief.

Osaka, this 29th day of June, 2006

Shin Tanimura

[Name of The Document] Description

[Title of the Invention] SCAN TEST CONTROL METHOD AND SCAN TEST

[CLAIMS]

[Claim 1] A scan test control method for a scan test circuit incorporating a scan chain having n pieces of scan storage elements (n: integer, n>1), wherein a frequency of a first clock to be used for shifting data into the first to (n-1)th scan storage elements, and a frequency of a second clock to be used for shifting data into the n-th scan storage element and performing normal operation, are independently controlled.

[Claim 2] The scan test control method of Claim 1, wherein the frequency of the first clock and the frequency of the second clock are different from each other.

[Claim 3] The scan test control method of Claim 1, wherein the frequency of the second clock is a frequency to be used in the normal operation.

[Claim 4] A scan test circuit comprising:

a scan chain having n pieces of scan storage elements (n: integer, n>1);

a scan clock generation circuit for receiving first and second clocks, and outputting an arbitrary clock as a scan clock; and

a selection circuit for using the first clock selectively for shifting data into the first to (n-1)th scan storage elements, and using the second clock selectively for shifting data into the

n-th scan storage element and performing normal operation.

[Claim 5] The scan test circuit of Claim 4 further including a scan selection signal generation circuit which receives, from the outside, a scan selection external signal, and generates a scan selection internal signal for selectively switching between the above-described normal operation and operation for shifting in synchronization with the second clock.

[Claim 6] The scan test circuit of Claim 5, wherein the scan selection signal generation circuit generates a control signal for generating an arbitrary number among the second clocks.

[Claim 7] The scan test circuit of Claim 6, wherein the scan selection signal generation circuit can switch between a first timing at which the scan clock generation circuit generates the second clock as the scan clock from the scan clock generation circuit, and a second timing at which the scan selection internal signal is generated.

[Claim 8] The scan test circuit of Claim 7, wherein the scan selection signal generation circuit can arbitrarily select one of the first timing and the second timing.

[Claim 9] The scan test circuit of Claim 8, wherein a storage element is provided in front of the scan chain.

[Claim 10] The scan test circuit of Claim 9, wherein

when generating a scan test pattern, the scan clock generation circuit is replaced with a circuit that connects the first clock directly to the scan clock,

the scan selection signal generation circuit is replaced with a circuit that connects a terminal to which the scan selection external signal is input, directly to a signal line from which the scan selection internal signal is output, and

the storage element is replaced with a circuit that connects a signal line to which data in the storage element is input, directly to a signal line from which the data is output.

[Claim 11] A scan test control method for a scan test circuit comprising a first block having a first scan test circuit that operates in synchronization with a first clock and a second clock, and a second block having a second scan test circuit that synchronizes only with the first clock, and the normal operation time of the scan test in the first block is different from the normal operation time of the scan test in the second block.

[Claim 12]A scan test circuit comprising a first block having a first scan test circuit that operates in synchronization with a first clock and a second clock, and a second block having a second scan test circuit that synchronizes only with the first clock, said scan test circuit comprising:

a plurality of first storage elements that synchronize with the first clock,

a plurality of second storage elements that synchronize with the first clock and the second clock,

a selection circuit for switching selectively either a first path between the plural first storage elements and the second

block, or a second path between the plural second storage elements and the first block, and

said first storage elements, second storage elements, and selection circuit being provided between the first block and the second block.

[Claim 13]The scan test circuit of Claim 12, wherein the plurality of first storage elements and the plurality of second storage elements are constituted by a plurality of controllable scan storage elements and a plurality of monitor storage elements.

[Claim 14]The scan test circuit of Claim 13, wherein the plurality of monitor storage elements can be bundled into a single monitor storage element.

[Claim 15]The scan test circuit of Claim 14, wherein the selection circuit can be replaced with a circuit which separates the first path and the second path, when generating a scan test pattern.

[Detailed Description of the Invention]

[0001]

[Technical Field of Invention]

The present invention relates to a scan test control method and a scan test circuit for detecting a stuck-at fault and a delay fault that occur in a semiconductor integrated circuit.

[0002]

[Prior Art]

In recent years, it has become possible to integrate several

millions of transistors in one chip, as semiconductor fine-patterning techniques have progressed. As one of test methods for such semiconductor integrated circuit, there is a scan test that ensures an extremely high rate of fault detection.

[0003]

Figure 18 is a block diagram illustrating a conventional scan test circuit. In figure 18, 111 denotes an external input terminal which receives a scan selection external signal for switching between normal operation and scan operation, 112 denotes an external input terminal which receives scan-in data, 114 denotes an external input terminal which receives a test clock, 119~121 denote normal data lines, 125~127 denote scan storage elements which hold the data in synchronization with the rising edge of the test clock inputted to the external input terminal 114, 122 denotes an output data line of the scan storage element 125, 123 denotes a data line of the scan storage element 126, 124 denotes an external output terminal which outputs the output data of the scan storage element 127. 118 denotes a combination circuit which receives from the output data lines 122 and 123, and outputs to the normal data lines 119~121. The scan test circuit shown in figure 18 tests the combination circuit 118.

[0004]

Figure 19 is a circuit diagram illustrating a concrete example of the scan storage elements 125~127. In figure 19, 3 denotes a normal data input terminal which receives normal data,

4 denotes a scan-in input terminal which receives scan-in data, 5 denotes a scan clock input terminal which receives a scan clock, 2 denotes a scan selection signal input terminal which selects normal data of the normal data input terminal and scan-in data of the scan-in input terminal, 1 denotes a selector circuit which outputs normal data of the normal data input terminal 3 when the scan selection external signal is "0", or outputs the scan-in data of the scan-in input terminal 4 when the scan selection external signal is "1", 6 denotes a storage element which holds and outputs the output signal of the selector circuit 1 in synchronization with the rising edge of the scan clock of the scan clock input terminal 5 and 7 denotes an output terminal which outputs the signal outputted from the storage element 6.

[0005]

Figure 20 is a time chart for explaining the operation of the scan test circuit constituted as described above. 1200～1204 denote scan-in data of the external input terminal 112, 1210～1212, 1250 and 1251 denote normal data on the normal data line 119, 1220～1222, 1260 and 1261 denote normal data on the normal data line 120, 1230～1232, 1270 and 1271 denote normal data on the normal data line 121, 1198 denotes initial data that is stored in the scan storage element 127 during scan operation, and 1199 denotes initial data that is stored in the scan storage element 126 during scan operation. Further, 350～355 denote event timings. Other reference numerals indicate the waveforms

of signals at the signal lines and external terminals corresponding to the reference numerals shown in figure 18.

[0006]

Hereinafter, the operation of the scan test circuit will be described with reference to figures 18~20. When the scan selection external signal of the external input terminal 111 is "0", the scan storage elements 125~127 are in the normal operation mode, and the normal operation is performed. That is, in synchronization with the rising edge of the test clock of the external input terminal 114, the scan storage element 125 holds and outputs the normal data supplied from the normal data line 119, the scan storage element 126 holds and outputs the normal data supplied from the normal data line 120, and the scan storage element 127 holds and outputs the normal data supplied from the normal data line 121. Therefore, the scan elements 125~127 serve as normal storage elements.

[0007]

When the scan selection external signal of the external input terminal 111 is "1", the scan storage elements 125~127 are in the scan mode, the scan operation is performed. That is, in synchronization with the rising edge of the test clock of the external input terminal 114, the scan storage element 125 holds and outputs the scan-in data inputted to the external input terminal 112, the scan storage element 126 holds and outputs the output data of the scan storage element 125, and the scan storage

element 127 holds and outputs the output data of the scan storage element 126. Therefore, the scan elements 125~127 serve as storage elements performing scan operation.

[0008]

Since the scan selection external signal of the external input terminal 11 is "1" at the event timing 350, the scan storage elements 125~127 are in the scan mode. The scan storage elements 125~127 synchronize with the rising edge of the test clock of the external input terminal 114, the scan storage element 125 holds and outputs the scan-in data 1201 of the external input terminal 112, the scan storage element 126 holds and outputs the output data 1200 of the scan storage element 125, and the scan storage element 127 holds and outputs the output data 1199 of the scan storage element 126. The external output terminal 124 outputs the output data 1199 of the scan storage element 127.

[0009]

Since the scan selection external signal of the external input terminal is "1" at the event timing 351, the scan storage elements 125~127 are in the scan mode. The scan storage elements 125~127 synchronize with the rising edge of the test clock of the external input terminal 114, the scan storage element 125 holds and outputs the scan-in data 1202 of the external input terminal 112, the scan storage element 126 holds and outputs the output data 1201 of the scan storage element 125,

and the scan storage element 127 holds and outputs the output data of the scan storage element 126. The external output terminal 124 outputs the output data 1200 of the scan storage element 127.

[0010]

The scan selection external signal of the external input terminal 111 transits to "0" at the event timing 352, and the scan storage elements 125~127 are switched into the normal operation mode.

[0011]

At the event timing 353, the scan storage elements 125~127, which are in the normal operation mode, synchronize with the rising edge of the test clock of the external input terminal 114, the scan storage element 125 holds and outputs the normal data 1212 supplied from the normal data line 119, the scan storage element 126 holds and outputs the normal data 1222 supplied from the normal data line 120, and the scan storage element 127 holds and outputs the normal data 1232 supplied from the normal data line 121. The external output terminal 124 outputs the output data 1232 of the scan storage element 127.

[0012]

At the event timing 354, the scan selection external signal of the external input terminal 111 transits to "1", and the scan storage elements 125~127 are switched into the scan mode.

[0013]

At the event timing 355, the scan storage elements 125~127, which are in the normal operation mode, synchronize with the rising edge of the test clock of the external input terminal 114, the scan storage element 125 holds and outputs the scan-in data 1204 supplied from the external input terminal 112, the scan storage element 126 holds and outputs the output data 1212 of the scan storage element 125, and the scan storage element 127 holds and outputs the output data 1222 of the scan storage element 126. The external output terminal 124 outputs the output data 1222 of the scan storage element 127.

[0014]

As described above, according to the conventional scan test circuit and scan test control method, in the scan test circuit incorporating the scan chain having the n pieces of scan storage elements (n: integer, n>0), the scan-in data are set in the scan storage element 125~127 of figure 8 in the scan mode, and the normal data of the normal data line 119~121 outputted from the combination circuit 118 in the normal operation mode are stored in the scan storage elements 125~127, respectively, and then the normal data stored in the scan storage elements 125~127 in the scan mode are scanned out to the external output terminal 124 to be observed, thereby detecting a fault in the semiconductor integrated circuit. (For example, refer to the unpantented reference 1.)

[0015]

[unpatented reference 1]

"Design of Testable Logic Circuit", written by R. G. Bennett, translated by Akemi Harada

[0016]

[Measures to solve the problem]

In the conventional scan test circuit and scan test control method, the scan-in data and the scan selection signal must be directly input to the scan storage elements in the semiconductor integrated circuit from the outside of the semiconductor integrated circuit, therefore, the rate of speed to the I/O of the semiconductor integrated circuit was limited, as the result, the scan test cannot be carried out as fast as the normal operation speed. Accordingly, in a semiconductor integrated circuit that ensures a high-speed frequency, the conventional scan test circuit and scan test control method cannot detect a delay fault that depends on the frequency while they can detect a stuck-at fault that does not depend on the frequency.

[0017]

The present invention is made in view of the above-described conventional problems and has for its object to provide a scan test circuit and a scan test control method that are able to detect not only a stuck-at fault but also a delay fault even when shift-in data and a scan selection external signal are supplied from the outside of a semiconductor integrated circuit as in the conventional scan test circuit and scan test control method.

[0018]

According to a first aspect of the present invention, a scan test control method incorporating a scan chain having n pieces of scan storage elements (n: integer, n>1), wherein a frequency of a first clock for shifting data into the first to (n-1)th scan storage elements, and a frequency of a second clock for shifting data into the n-th scan storage element and performing normal operation, are independently controlled. Therefore, it is possible to realize compatibility between a stable scan operation of inputting shift-in data into the scan storage elements and a normal operation, which results in effective detection of a delay fault as well as effective detection of a stuck-at fault in a semiconductor integrated circuit.

[0019]

According to a second aspect of the present invention, in the scan test control method according to the first aspect, the frequency of the first clock and the frequency of the second clock are different from each other.

[0020]

According to a third aspect of the present invention, in the scan test control method according to the first aspect, the frequency of the second clock is the normal operation frequency.

[0021]

According to a fourth aspect of the present invention, there is provided a scan test circuit comprising: a scan chain having n

pieces of scan storage elements (n: integer, n>1); a scan clock generation circuit for outputting first and second clocks as inputs, and an arbitrary clock as a scan clock; and a selection circuit for using input of the first clock selectively for shifting data into the first to (n-1)th scan storage elements, and using input of the second clock selectively for shifting data into the n-th scan storage element and performing normal operation. Therefore, it is possible to realize compatibility between a stable scan operation of inputting shift-in data into the scan storage elements and a normal operation, which results in effective detection of a delay fault as well as effective detection of a stuck-at fault in a semiconductor integrated circuit.

[0022]

According to a fifth aspect of the present invention, the scan test circuit according to the fourth aspect further includes a scan selection signal generation circuit which receives, from the outside, a scan selection external signal, and generates a scan selection internal signal for selectively switching between normal operation and operation for shifting data in synchronization with the second clock.

[0023]

According to a sixth aspect of the present invention, in the scan test circuit according to the fifth aspect, the scan selection signal generation circuit generates a control signal

for generating an arbitrary number among the second clocks.

[0024]

According to a seventh aspect of the present invention, in the scan test circuit according to the sixth aspect, the scan selection signal generation circuit can switch between a first timing at which the scan clock generation circuit generates the second clock as the scan clock, and a second timing at which the scan selection internal signal is generated.

[0025]

According to an eighth aspect of the present invention, in the scan test circuit according to the seventh aspect, the scan selection signal generation circuit can arbitrarily select the first timing or the second timing.

[0026]

According to a ninth aspect of the present invention, in the scan test circuit according to the eighth aspect, a storage element is provided in front of the scan chain. Therefore, the data stored in the scan storage elements during the normal operation become identical to those stored during the conventional scan test, whereby the shift-in data in the conventional scan test can be scan-tested as they are. Further, the detection rate of stuck-at fault in a semiconductor integrated circuit can be equal to that in the conventional scan test.

[0027]

Further, according to a tenth aspect of the present invention, in the scan test circuit according to the ninth aspect, when generating a scan test pattern, the scan clock generation circuit can be switched with a circuit that connects the first clock directly to the scan clock; the scan selection signal generation circuit can be switched with a circuit that connects the scan selection external signal directly to the scan selection internal signal; and the storage element can be switched with a circuit that connects an input of the storage element directly an output. Therefore, even when there is a scan design protocol defining that a scan selection external signal supplied from the outside of a semiconductor integrated circuit must be the same as a scan selection internal signal, and scan-in data supplied from the outside of the semiconductor integrated circuit and scan-in data inputted to scan storage elements must be synchronized with each other by a single clock, it is possible to generate a scan test pattern without infringing the scan design protocol, which results in effective detection of a delay fault as well as effective detection of a stuck-at fault in the semiconductor integrated circuit.

[0028]

Further, according to an eleventh aspect of the present invention, a scan test control method comprises a first block having a first scan test circuit that operates in synchronization with a first clock and a second clock, and a second block having

a second scan test circuit that is synchronized with only the first clock, wherein the normal operation time of the scan test in the first block is different from the normal operation time of the scan test in the second block. Therefore, passing of desired data between the first block and the second block becomes possible, whereby the first block and the second block can be simultaneously subjected to scan test, and further, a stuck-at fault between the first block and the second block can also be detected.

[0029]

Further, according to a twelfth aspect of the present invention, there is provided a scan test circuit having a first block having a first scan test circuit that operates in synchronization with a first clock and a second clock, and a second block having a second scan test circuit that is synchronized only with the first clock, and the scan test circuit comprises: a plurality of first storage elements synchronized with the first clock; a plurality of second storage elements synchronized with the first clock and the second clock; and a selection circuit for selectively switching either a first path between the plural first storage elements and the second block, or a second path between the plural second storage elements and the first block, as a path for passing data from the first block to the second block. Therefore, passing of desired data between the first block and the second block becomes possible, whereby

the first block and the second block can be simultaneously subjected to scan test, and further, a stuck-at fault between the first block and the second block can also be detected.

[0030]

Further, according to a thirteenth aspect of the present invention, in the scan test circuit according to the twelfth aspect, the plurality of first storage elements and the plurality of second storage elements are constituted by a plurality of controllable scan storage elements and a plurality of monitor storage elements.

[0031]

Further, according to a fourteenth aspect of the present invention, in the scan test circuit according to the thirteenth aspect, the plurality of monitor storage elements can be bundled into a single monitor storage element.

[0032]

According to a fifteenth aspect of the present invention, in the scan test circuit according to the fourteenth aspect, the selection circuit is replaced with a circuit which separates the first path from the second path, when generating a scan test pattern. Therefore, between the first block and the second block, a scan test pattern can be generated for each of the first path between the storage elements which are synchronized with the first clock, and the second path between the storage elements which are synchronized with the scan clock generated by the scan

clock generation means, and the scan test using the scan test control method or the scan test circuit according to any of the eleventh to fourteenth aspects can be carried out using the scan pattern thus generated.

[0033]

From the aspects described above, the scan test circuit and the scan test control method can detect a stuck-at fault equivalent to the conventional scan test circuit and scan test control method, and further, possible to detect a delay fault.

[0034]

[Embodiments of the invention]

Hereinafter, preferred embodiments of the present invention will be described with reference to the drawings.

[Embodiment 1]

Figure 1 is a block diagram illustrating a scan test circuit according to a first embodiment of the present invention. In figure 1, 12 denotes an external input terminal which receives scan-in data, 13 denotes an external input terminal which receives a normal operation clock, 16 denotes a scan selection internal signal line for switching the normal operation mode and the scan mode, 17 denotes a scan clock signal line, 15 denotes a scan control circuit which receives the scan selection external signal from the external input terminal 11, the normal operation clock from the external input terminal 13, and the test clock from the external input terminal 14, and generates a scan

selection internal signal and outputs to the scan selection internal signal line 16, also generates a scan clock and outputs to the scan clock signal line 17, 19~21 denote normal data lines, 25~27 denote scan storage elements which synchronize with the rising edge of the scan clock that is generated by the scan control circuit 15, 22 denotes an output data line of the scan storage element 25, 24 denotes an external output terminal which outputs output data of the scan storage element 27, 18 denotes a combination circuit which receives the data from the output data lines 22 and 23, and outputs the data to the normal data lines 19 ~21.

[0035]

Figure 2 is a block diagram illustrating a concrete example of the scan control circuit 15 shown in figure 1. The same reference numerals as those shown in figure 1 denote the same or corresponding parts. In figure 2, 32 denotes a normal operation clock mask signal line, 42 denotes an output signal, 31 denotes a scan selection internal signal generation circuit which receives a scan selection external circuit received from the external input terminal 11, a normal operation clock received from the external input terminal 13 and a test clock received from the external input terminal 14 as inputs and outputs a signal generated by the circuit to the scan selection internal signal line 16, the normal clock mask signal line 32 and the output signal line 42, 33 denotes a scan clock generation circuit which

receives a scan selection external signal received from external input terminal 11, a normal operation clock received from the external input terminal 13, a test clock received from the external terminal 14, a normal operation clock mask signal of the normal operation clock mask signal line 32 and a signal of the output signal line 42 as inputs and outputs a signal generated by the terminal to the scan clock signal line as the clocks of the scan storage elements 19~21.

[0036]

Figure 3 is a block diagram illustrating a concrete example of the scan selection internal signal generation circuit 31 shown in figure 2. The same reference numerals as those shown in figure 2 denote the same or corresponding parts. In figure 3, 41 denotes a storage element which holds and outputs a scan selection external signal inputted to the external input terminal 11, in synchronization with the rising edge of the test clock received by the external input terminal 14, 42 denotes an output signal line of the storage element 41, 44 denotes an inverter circuit, 43 denotes an output signal line of the inverter circuit 44, 45 denotes an m-stage shift register which holds the signal supplied from the output signal line 42, in synchronization with the rising edge of the normal operation clock inputted from the external input terminal 13, 47 denotes an EXNOR circuit 49 which outputs a signal "1" when the signal from the output signal line 47 matches the signal from the output signal line 48, and outputs

a signal "0" when these signals do not match, 52 denotes an output signal line of the EXNOR circuit 49, 50 denotes a latch circuit which outputs the signal supplied from the output signal line 52 as it is when the normal operation clock is in negative logic, and holds the signal supplied from the output signal line at the rising edge of the normal operation clock, 32 denotes a normal operation mask signal line for outputting the output signal of the latch circuit 50 as a normal operation mask signal. 51 denotes a storage element which holds a signal that is obtained by inverting the logic value of the signal from the normal operation mask signal line 32, in synchronization with the falling edge of the normal operation clock received by the external input terminal 13, 53 denotes an output data line of the storage element 51, and 54 denotes an OR circuit which receives the signal from the output signal line 47 and the signal from the output signal line 53, and outputs them to the scan selection internal signal line 16.

[0037]

Figure 4 is a block diagram illustrating a concrete example of the scan clock generation circuit 33 shown in figure 2. In figure 4, 61 denotes an AND circuit which receives the normal operation clock from the external input terminal 13, and the normal operation mask signal from the normal operation mask signal line 32, and outputs a normal operation clock, 63 denotes an AND circuit which receives the test clock from the external

input terminal 14, and the scan selection external signal from the external input terminal 11, and outputs the test clock, 64 denotes an output signal line of the AND circuit 63, 65 denotes a selector circuit which outputs, as a scan clock, the normal operation clock supplied from the output signal line 62, to the scan clock signal line 17, when the signal supplied from the output signal line 42 is "0", and outputs the test clock supplied from the output signal line 64, to the scan clock signal line 17, when the signal supplied from the output signal line 42 is "1".

[0038]

Figure 5 is a block diagram illustrating a concrete example of the m-stage shift register shown in figure 3. In figure 5, 70 denotes a storage element 41 which holds the scan selection external signal of the external input terminal 42 and outputs it to the output signal line 47 in synchronization with the rising of the test clock of the external input terminal 14.

[0039]

Figure 6 is a block diagram illustrating a concrete example of the (m+2)-stage shift register shown in figure 3. The same reference numerals as those shown in figure 3 denote the same parts. In figure 6, 71 denotes a storage element which holds and outputs the signal of the external signal line 43 in synchronization with the rising of the normal operation clock of the external input terminal 13, 72 denotes a storage element which holds and outputs the output signal of the storage element

71 in synchronization with the rising of the normal operation clock of the external input terminal 13, 73 denotes a storage element which holds the output signal of the storage element 72 and outputs to the output signal line 48 in synchronization with the rising of the normal operation clock of the external input terminal 13.

[0040]

Figure 7 is a time chart for explaining the operation of the scan test circuit constituted as described above. In figure 7, 200～204 denote scan-in data inputted to the external input terminal 12, 210～215 denote normal data of the normal data line 19, 220～225 denote normal data of the normal data line 20, 230～235 denote normal data of the normal data line 21, 198 denotes initial data that is stored in the scan storage element 27 during the scan operation, and 199 denotes initial data stored in the scan storage element 26 during the scan operation. Further, 300～313 denote event timings. Other reference numerals indicate the waveforms of signals at the signal lines and external terminals corresponding to those shown in figures 1 to 6.

[0041]

Hereinafter, the operation of the scan test circuit will be described with reference to figures 1～7. It is assumed that the normal operation clock of the external input terminal 13 is six times as high as the test clock of the external input terminal 14. Further, it is assumed that m is equal to 1, and "1" is stored in

the storage elements 41, 51, and 70 while "0" is stored in the storage elements 71, 72, 73 and the latch circuit 50, as initial values.

[0042]

When the signal from the scan selection internal signal line 16 is "0", the scan storage elements 25~27 are in the normal operation mode and the normal operation is performed. That is, in synchronization with the rising edge of the scan clock of the scan clock signal line 17, the scan storage element 25 holds and outputs the normal data supplied from the normal data line 19, the scan storage element 26 holds and outputs the normal data supplied from the normal data line 20, and the scan storage element 27 holds and outputs the normal data supplied from the normal data line 21. Therefore, the scan storage elements 25~27 serve as normal storage elements.

[0043]

When the signal from the scan selection internal signal line 16 is "1", the scan storage elements 25~27 are in the scan mode and the scan operation is performed. That is, in synchronization with the rising edge of the scan clock of the scan clock signal line 17, the scan storage element 25 holds and outputs the scan-in data supplied from the external input terminal 12, the scan storage element 26 holds and outputs the output data of the scan storage element 25, and the scan storage element 27 holds and outputs the output data of the scan storage element 26. Therefore,

the scan storage elements 25~27 serve as storage elements.

[0044]

At the event timing 300, the storage element 41 holds the scan selection external signal "1" of the external input device and outputs it to the output signal line 42 in synchronization with the rising edge of the test clock of the external input terminal 14. However, the values of the storage element 41 are not changed. At this time, the selector circuit 65 selects the output signal line 64 from the "1" signal of the output signal line 42, and the AND circuit 63 outputs the test clock of the external input terminal 14 to the output signal line 64 because the scan selection external signal remains "1". Accordingly, the signal of the scan clock signal line 17 becomes a test clock of the external input terminal.

[0045]

Further, the values of the storage element 51, the storage elements 70~73, and the latch circuit 50 are not changed like those of the storage element 41. Accordingly, the scan selection signal from the scan selection signal line 16 remains "1", whereby the scan storage elements 25~27 go into the scan mode. the scan storage elements 25~27 synchronize with the rising of the test clock of the external input terminal 14, the scan storage element 25 holds and outputs the scan-in data 201 of the external input terminal 12, the scan storage element 26 holds and outputs the output data 200 of the scan storage element 25, and

the scan storage element 27 holds and outputs the output data 199 of the scan storage element 26. The external output terminal 24 outputs the output data 199 of the scan storage element 27. That is, the scan operation at the event timing 300 performs scan-in and scan-out using the test clock.

[0046]

Since, at the event timing 301, the scan selection external signal of the external input terminal 11 remains "1" as at the event timing 300, the signal from the scan clock signal line 17 becomes a test clock of the external input terminal 14. Further, since the value of the scan selection signal line 16 remains "1", the scan storage elements 25~27 go into the scan mode. The scan storage elements 25~27 synchronize with the rising of the test clock, the scan storage element 25 holds and outputs the scan-in data 202 supplied from the external input terminal 12, the scan storage element 26 holds and outputs the output data 201 of the scan storage element 25, and the scan storage element 27 holds and outputs the output data 200 of the scan storage element 26. The external output terminal 24 outputs the output data 200 of the scan storage element 27. That is, the scan operation at the event timing 301 performs scan-in and scan-out using the test clock.

[0047]

At the event timing 302, the scan selection external signal of the external input terminal 11 transits to "0". Therefore,

the AND circuit 63 outputs "0" to the output signal line 64, and maintains the scan clock of the scan clock signal line 17 at "0" through the selector circuit 65.

[0048]

At the event timing 303, the storage element 41 holds "0" of the scan selection external signal of the external input terminal and outputs it to the output signal line 42 in synchronization with the rising of the test clock of the external input terminal 14. Further, the inverter circuit 44 receives the output value "0" supplied from the storage element 41, and outputs "1" to the output signal line 43. The selector circuit 65 selects the output signal line 62 because the signal of the output signal line 42 becomes "0", and outputs to the scan clock signal line 17. At this time, because the signal supplied from the normal operation clock mask signal line 32 is "0", the normal operation clock of the external input terminal 13 is masked by the AND circuit 61, thereby the signal line 62 is "0". Accordingly, the scan clock from the scan clock signal line 17 remains "0".

[0049]

At the event timing 304, the storage element 70 in the m-stage shift register 45 holds and outputs "0" of the output signal of the storage element 41 in synchronization with the rising edge of the normal operation clock of the external input terminal 13. Further, in synchronization with the rising of the normal operation clock of the external input terminal 13, the

storage element 71 in the (m+2)-stage shift register 46 holds and outputs the signal "1" supplied from the output signal line 43, the storage element 72 holds and outputs "0" of the output signal of the storage element 71, and the storage element 73 holds and outputs the output signal "0" of the storage element 72. Then, the EXNOR circuit 49 receives the signal "0" from the output signal line 47 and the signal "0" from the output signal line 48, and outputs "1" to the output signal line 52.

[0050]

At the event timing 305, the storage element 51 holds and outputs the inverted value "1" of "0" of the output signal is supplied from the latch circuit 50, in synchronization with the falling edge of the normal operation clock of the external input terminal 13. At this time, because the signal supplied from the output signal line 47 is "0", the OR circuit 54 outputs the output signal "1" of the storage element 51 to the scan selection internal signal line 16. However, the value of the scan selection internal signal supplied from the scan selection internal signal line 16 is not changed. On the other hand, the latch circuit 50 outputs the signal "1" supplied from the output signal line 52 to the normal operation clock mask signal line 32 at the falling edge of the normal operation clock of the external input terminal 13. Thereby, the AND circuit 61 outputs the normal operation clock of the external input terminal 13 to the output signal line 62, and the selector circuit 65 outputs the

signal supplied from the output signal line 62, to the scan clock signal line 17. Thereby, the signal supplied from the scan clock signal line 17 becomes the normal operation clock.

[0051]

At the event timing 306, the storage element 70 in the m-stage shift register 45 holds "0" of the output signal of the storage element 41 and outputs it to the output signal line 47 in synchronization with the rising edge of the normal operation clock the external input terminal 13, but the value is not changed. Further, the storage element 71 in the (m+2)-stage shift register 46 holds and outputs the signal "1" supplied from the output signal line 43, the storage element 72 holds and outputs the output signal "1" of the storage element 71, and the storage element 73 holds and outputs the output signal "0" of the storage element 72, in synchronization with the rising edge of the normal operation clock of the external input terminal 13. Then the EXNOR circuit 49 receives the signal "0" supplied from the output signal line 47 and the signal "0" supplied from the output signal line 48, and outputs the signal "1" to the output signal line 52, but the value is not changed. On the other hand, since the signal on the scan selection internal signal line 16 is maintained at "1", the scan storage element 25~27, which are in the scan mode, synchronize with the rising of the normal operation clock of the scan clock signal line 17, the scan storage element 25 holds and outputs the scan-in data 203

supplied the external input terminal 12, the scan storage element 26 holds and outputs the output data 202 of the scan storage element 25, and the scan storage element 27 holds and outputs the output data 201 of the scan storage element 26. The external output terminal 24 outputs the output data 201 of the scan storage element 27. That is, the final scan operation at the event timing 306 performs scan-in and scan-out using the normal operation clock.

[0052]

At the even timing 307, the storage element 51 holds and outputs the inverted value "0" of the output signal "1" supplied from the latch circuit 50, in synchronization with the falling edge of the normal operation clock of the external input terminal 13. At this time, since the signal on the output signal line 47 is "0", the OR circuit 54 outputs the output signal "0" of the storage element 51 to the scan selection internal signal line 16. Therefore, the scan storage elements 25~27 are changed from the scan mode to the normal operation mode.

[0053]

At the event timing 308, the scan selection external signal of the external input terminal 11 transits to "1". Therefore, the AND circuit 63 outputs the test clock of the external input terminal 14 to the output signal line 64, but the test clock does not adversely affect the scan clock signal line 17 because the selector circuit 65 selects the output signal line 62. On the

other hand, the storage element 70 in the m-stage shift register 45 holds and outputs the output signal "0" of the storage element 41 in synchronization with the rising edge of the normal operation clock of the external input terminal 13. Further, in synchronization with the rising edge of the normal operation clock the external input terminal 13, the storage element 71 in the (m+2)-stage shifter register 46 holds and outputs "1" of the signal supplied from the output signal line 43, the storage element 72 holds and outputs the output signal "1" of the storage element 71, and the storage element 73 holds and outputs the output signal "1" of the storage element 72. Then, the EXNOR circuit 49 receives the signal "0" supplied from the output signal line 47 and the signal "1" supplied from the output signal line 48, and outputs "0" to the output signal line 52. As for the scan storage elements 25～27 which are switched to the normal operation mode, the scan storage element 25 holds and outputs the normal data 213 supplied from the normal data line 19, the scan storage element 26 holds and outputs the normal data 223 supplied from the normal data line 20, and the scan storage element 27 holds and outputs the normal data 233 supplied from the normal data line 21, in synchronization with the rising edge of the normal operation clock of the external input terminal 13. The normal operation at the event timing 308 carries out using the normal operation clock.

[0054]

At the event timing 309, the storage element 51 holds and outputs the inverted value "0" of "1" of the output signal supplied from the latch circuit 50, in synchronization with the falling edge of the normal operation clock of the external input terminal 13. At this time, since the signal supplied from the output signal line 47 is "0", the OR circuit 54 outputs the output signal "0" of the storage element 51 to the scan selection internal signal line 16. However, the value of the signal supplied from the scan selection internal signal line 16 is not changed. On the other hand, the latch circuit 50 outputs the signal "0" supplied from the output signal line 52, to the normal operation clock mask signal line 32, at the falling edge of the normal operation clock of the external input terminal 13. The AND circuit 61 outputs the signal "0" to the output signal line 62, and masks the normal operation clock.

[0055]

At the event timing 310, the storage element 51 holds and outputs the inverted value "1" of the output signal "0" supplied from the latch circuit 50, in synchronization with the falling edge of the normal operation clock of the external input terminal 13. Since the signal supplied from the output signal line 47 at this time is "0", the OR circuit 54 outputs the output signal "1" of the storage element 51 to the scan selection internal signal line 16. Therefore, the scan storage elements 25~27 are changed from the normal operation mode to the scan mode. On the other

hand, the latch circuit 50 outputs the signal "0" supplied from the output signal line 52, to the normal operation clock mask signal line 32 at the falling edge of the normal operation clock of the external input terminal 13. However, the value is not changed.

[0056]

At the event timing 311, the storage element 41 holds the scan selection external signal "1" of the external input terminal 11 and outputs it to the output signal line 42 in synchronization with the rising edge of the test clock. Further, the inverter circuit 44 receives the output signal "1" from the storage element 41, and outputs the signal "0" to the output signal line 43. The selector circuit 65 selects the signal supplied from the output signal line 64 and outputs it to the scan clock signal line 17 because the signal supplied from the output signal line 42 is "1". At this time, the AND circuit 63 outputs the test clock to the output signal line 64 because the scan selection external signal of the external input terminal is "1". Accordingly, the scan clock supplied from the scan clock signal line 17 becomes a test clock. The scan storage elements 25~27 synchronize with the rising edge of the test clock, the scan storage element 25 holds and outputs the scan-in data 204 supplied from the external input terminal 12, the scan storage element 26 holds and outputs the output data 213 of the scan storage element 25, and the scan storage element 27 holds and

outputs the output data 223 of the scan storage element 26. The external output terminal 24 outputs the output data 223 of the scan storage element 27. That is, the scan operation at the event timing 311 performs scan-in and scan-out using the test clock.

[0057]

At the event timing 312, the storage element 70 in the m-stage shift register 45 holds the output signal "1" of the storage element 41 and outputs it to the output signal line 42 in synchronization with the rising edge of the normal operation clock of the external input terminal 13. Further, the storage element 71 in the (m+2)-stage shift register 46 holds and outputs the signal "0" supplied from the output signal line 43, the storage element 72 holds and outputs the output signal "1" of the storage element 71, and the storage element 73 holds and outputs the output signal "1" of the storage element 72. Then, the EXNOR circuit 49 receives the signal "1" from the output signal line 47 and the signal "1" from the output signal line 48, and outputs the signal "1" to the output signal line 52.

[0058]

At the event timing 313, the storage element 51 holds and outputs the inverted value "1" of the output signal "0" from the latch circuit 50 in synchronization with the falling edge of the normal operation clock of the external input terminal 13. At this time, because the signal from the output signal line 47 is

"1", the OR circuit 54 outputs the output signal "1" of the storage element 51 to the scan selection internal signal line 16. Therefore, the value of the signal from the scan selection internal signal line 16 is not changed, and the scan storage elements 25～27 remain in the scan mode. On the other hand, the latch circuit 50 outputs the signal "1" supplied from the output signal line 52, to the normal operation clock mask signal line 32 at the falling edge of the normal operation clock of the external input terminal 13. Accordingly, the AND circuit 61 outputs the normal operation clock to the output signal line 62. However, the selector circuit 65 selects the signal of the output signal line 64 and outputs it to the scan clock signal line 17 because the signal from the output signal line 42 is maintained at "1". Accordingly, the signal of the scan clock signal line 17 remains as a test clock.

[0059]

With respect to the operation described above, the outline of the processing for generating a test line using the first embodiment of the invention will be described with reference to a flowchart shown in figure 8. In figure 8, 800～812 denote steps.

[0060]

(1) Processing at steps 800～802

The scan test circuit of the first embodiment receives the test clock of the external input terminal 14, the normal operation clock of the external input terminal 13, and the scan

selection external signal of the external input terminal 11. The scan control circuit 15 switches the scan clock from the scan clock signal line 17 to the test clock of the external input terminal 14, and generates the scan selection internal signal of the scan selection internal signal line 16 from the scan selection external signal of the external input terminal 11, thereby setting the n (n=3) pieces of scan storage elements 25～27 in the scan mode.

[0061]

(2) Processing at step 803

It is judged whether the scan-in data is stored in the (n-1)th scan storage element 26 or not. In figure 7, at the event timing 300, the result of judgement is "NO" because the scan-in data 201 has not yet been stored in the scan storage element 26, and the processing goes to step 804.

[0062]

(3) Processing at step 804

The scan storage elements 25 and 26 hold and output the scan-in data of the external input terminal 12, in synchronization with the rising edge of the test clock of the external input terminal 14.

[0063]

(4) Processing at step 803

It is judged whether the scan-in data is stored in the (n-1)th scan storage element 26 or not. In figure 7, at the event

timing 301, the result of judgement is "YES" because the scan-in data 201 is stored in the scan storage element 26, and the processing goes to step 805.

[0064]

(5) Processing at step 805

In figure 7, at the event timing 302, the scan selection external signal of the external input terminal 11 is switched to the normal operation mode. However, the scan control circuit 15 maintains the scan selection internal signal from the scan selection internal signal line 16 in the current scan mode. Accordingly, the n (n=3) pieces of scan storage elements 25～27 remain in the scan mode.

[0065]

(6) Processing at step 806

In figure 7, at the event timing 303, the scan control circuit 15 changes the scan clock supplied from the scan clock signal line 17 to the normal operation clock of the external input terminal 13. However, the scan control circuit 15 masks the normal operation clock to prevent the clock from entering into the n pieces of scan storage elements 25～27.

[0066]

(7) Processing at step 807

The scan control circuit 15 unmasks the normal operation clock, and the n pieces of scan storage elements 25～27 hold and output the scan-in data supplied from the external input terminal

12 in synchronization with the normal operation clock, at the event timing 307, as shown in figure 7.

[0067]

(8) Processing at step 808

In figure 7, at the event timing 307, the scan control circuit 15 switches the scan selection internal signal from the scan selection internal signal line 16 to the normal operation mode.

[0068]

(9) Processing at step 809

In figure 7, at the event timing 308, the n (n=3) pieces of scan storage elements 25~27 hold and output the normal data in synchronization with the normal operation clock. At this time, the scan selection external signal of the external input terminal 11 is switched to the scan mode, but the scan control circuit 15 maintains the scan selection internal signal from the scan selection internal signal line 16 in the normal operation mode.

[0069]

(10) Processing at step 810

In figure 7, at the event timing 310, the scan control circuit 15 switches the scan selection internal signal from the scan selection internal signal line 16 to the scan mode. Further, at the event timing 311, the scan control circuit 15 switches the scan clock from the scan clock signal line 17 to the test clock of the external input terminal 14.

[0070]

(11) Processing at step 811

In this step, it is judged whether the processing is ended or not. When the scan-in data to be tested still remain, the judgement is "NO", and the processing goes to step 803 to repeat the above-described processing. When there remain no scan-in data to be tested, the judgement is "YES", and the processing goes to step 812.

[0071]

(12) Processing at step 812

All of the normal data stored in the n (n=3) pieces of scan storage elements 25~27 in step 809 are output to the external output terminal 24 in synchronization with the test clock of the external input terminal 14, thereby ending the processing.

[0072]

As described above, the scan test circuit according to the first embodiment of the present invention is incorporated with the scan chain having n pieces of scan storage elements (n: integer, n>1), and the frequency of the first clock for shifting data into the first to (n-1)th scan storage elements and the frequency of the second clock for shifting data into the n-th scan storage element and performing the normal operation are independently controlled, whereby compatibility between the stable scan operation of inputting the shift-in data into the scan storage elements and the normal operation can be realized,

which results in effective detection of a delay fault as well as effective detection of a stuck-at fault.

[0073]

[Embodiment 2]

In the scan test of the first embodiment of the present invention, the number is increased by one time compared with scan operations of the conventional scan test. This is evident from comparison between the timing chart in figure 20 of the conventional scan test and the timing chart in figure 7. In the conventional scan test, as shown in figure 20, the scan storage elements 125~127 perform the last scan operation at the event timing 351, and the scan storage elements 125~127 perform the normal operation at the event timing 353 after the scan selection external signal at the external input terminal 111 is changed to "0". However, in the scan test of the first embodiment of the present invention, as shown in figure 7, the scan storage elements 25~27 perform the last but one scan operation at the event timing 301, and the scan storage elements 25~27 do not yet perform the last scan operation at the event timing 353 after the scan selection external signal at the external input terminal 11 is changed to "0". The scan storage elements 25~27 perform the last scan operation at the event timing 306. That is, when the shift-in data of the conventional scan test is applied as it is to the scan test of the first embodiment of the present invention, the number of scan operations increases by one. Thereby, the

data stored in the scan storage elements 25~27 during the normal operation are undesirably different from the data in the conventional scan test. So, in this second embodiment of the present invention, a desired circuit is added to the scan chain comprising the scan storage elements 25~27 so that the data stored in the scan storage elements 25~27 during the normal operation become the same as the data in the conventional scan test.

[0074]

Figure 10 is a block diagram illustrating a scan test circuit according to the second embodiment. In figure 10, 28 denotes a storage element ,which is newly added this time, and 29 denotes an output signal line. Other constituents are identical to those of the scan test circuit according to the first embodiment.

[0075]

Figure 11 is a time chart for explaining the operation of the scan test circuit constructed as described above. In figure 11, the same reference numerals as those shown in figure 7 denote the same parts. 400~403 denote normal data on the normal data line 19, 410~413 denote normal data on the normal data line 20, 420~423 denote normal data on the normal data line 21, and 180 denotes initial data that is stored in the scan storage element 25 during the scan operation. Further, 360~364 denote event timings. Other reference numerals indicate the waveforms of

signals at the signal lines and external terminals corresponding to the reference numerals shown in figures 1~6 and 10.

[0076]

Hereinafter, the operation of the scan test circuit will be described with respect to only the data stored in the storage element 28 and the scan storage elements 25~27, with reference to figures 10 and 11. Since the operations of other elements are identical to those described for the first embodiment, it is substituted with the description of the first embodiment.

[0077]

At the event timing 360, the storage element 28 holds and outputs the scan-in data 201 inputted to the external input terminal 12, in synchronization with the rising edge of the test clock of the external input terminal 14. With respect to the scan storage elements 25~27 ,which are in the scan mode, the scan storage element 25 holds and outputs the output data 200 of the storage element 28 in synchronization with the rising edge of the test clock of the external input terminal 12. The scan storage element 26 holds and outputs the output data 200 of the storage element 25 in synchronization with the rising edge of the test clock of the external input terminal 14. The scan storage element 27 holds and outputs the output data 199 of the scan storage element 26 in synchronization with the rising edge of the test clock of the external input terminal 14. The external output terminal 24 outputs the output data 199 of the scan

storage element 27.

[0078]

At the event timing 361, the storage element 28 holds and outputs the scan-in data 202 supplied from the external input terminal 12, in synchronization with the rising edge of the test clock of the external input terminal 14. With respect to the scan storage elements 25~27 ,which are in the scan mode, the scan storage element 25 holds and outputs the output data 201 of the storage element 28 in synchronization with the rising edge of the test clock of the external input terminal 14. The scan storage element 26 holds and outputs the output data 200 of the storage element 25 in synchronization with the rising edge of the test clock of the external input terminal 14. The scan storage element 27 holds and outputs the output data 180 of the scan storage element 26 in synchronization with the rising edge of the test clock of the external input terminal 14. The external output terminal 24 outputs the output data 180 of the scan storage element 27.

[0079]

At the event timing 362, the storage element 28 holds and outputs the scan-in data 203 of the external input terminal 12 in synchronization with the rising edge of the normal operation clock of the external input terminal 13. With respect to the scan storage elements 25~27 ,which are in the scan mode, the scan storage element 25 holds and outputs the output data 202 of

the storage element 28 in synchronization with the rising edge of the normal operation clock of the external input terminal 13. The scan storage element 26 holds and outputs the output data 201 of the scan storage element 25 in synchronization with the normal operation clock. The scan storage element 27 holds and outputs the output data 200 of the scan storage element 26 in synchronization with the rising edge of the normal operation clock. The external output terminal 24 outputs the output data 200 of the scan storage element 27. At this time, since the scan storage elements 25~27 hold the same data as those held at the event timing 351 in the conventional scan test shown in figure 20, the normal data on the normal data lines 19~21 become equal to those at the event timing 351. To be specific, the normal data on the normal data line 19 is data 212, the normal data on the normal data line 20 is data 222, and the normal data on the normal data line 21 is data 232.

[0080]

At the event timing 363, the storage element 28 holds and outputs the scan-in data 203 in synchronization with the rising edge of the normal operation clock of the external input terminal 13. With respect to the scan storage elements 25~27 ,which are in the normal operation mode, the scan storage element 25 holds and outputs the normal data 212 supplied from the normal data line 19 in synchronization with the rising edge of the normal operation clock of the external input terminal 13. The scan

storage element 26 holds and outputs the normal data 222 supplied from the normal data line 20 in synchronization with the rising edge of the normal operation clock of the external input terminal 13. The scan storage element 27 holds and outputs the normal data 232 supplied from the normal data line 21 in synchronization with the rising edge of the normal operation clock of the external input terminal 13. The external output terminal 24 outputs the output data 232 of the scan storage element 27.

[0081]

At the event timing 364, the storage element 28 holds and outputs the scan-in data 204 of the external input terminal 12, in synchronization with the rising edge of the test clock of the external input terminal 14. With respect to the scan storage elements 25~27 ,which are in the scan mode, the scan storage element 25 holds and outputs the output data 203 of the storage element 28 in synchronization with the rising edge of the test clock of the external input terminal 14. The scan storage element 26 holds and outputs the output data 212 of the scan storage element 25 in synchronization with the rising edge of the test clock of the external input terminal 14. The scan storage element 27 holds and outputs the output data 222 of the scan storage element 26 in synchronization with the rising edge of the test clock of the external input terminal 14. The external output terminal 24 outputs the output data 222 of the scan storage element 27.

[0082]

According to the scan test circuit and the scan test control method according to the second embodiment of the present invention, since additional the storage element is provided in front of the scan chain having the n pieces of scan storage elements, the data stored in the scan storage elements during the normal operation are equal to those in the conventional scan test, and the shift-in data of the conventional scan test can be applied. Further, the effect of the detection rate of stuck-at fault in the semiconductor integrated circuit being maintained can be obtained.

[0083]

[Embodiment 3]

In the second embodiment, since the data stored in the scan storage elements during the normal operation are the same as those in the conventional scan test, it is possible to apply the scan-in data in the conventional scan test as they are. However, when generating a scan test pattern, if there is a scan design protocol that the scan selection external signal supplied from the outside of the semiconductor integrated circuit must be the same as the scan selection internal signal, and the scan-in data supplied from the outside of the semiconductor integrated circuit and the scan-in data inputted to the scan storage elements must be synchronized with each other by a single clock, the scan test circuit according to the second embodiment is against the scan

design protocol. So, in the scan test circuit of the third embodiment, the scan control circuit 15 and the storage element 28 are replaced with other circuits when generating a scan test pattern so that the circuit construction becomes the same as that of the conventional scan test circuit, thereby preventing the scan test circuit from infringing the scan design protocol.

[0084]

Figure 12 is a block diagram illustrating the scan test circuit according to the third embodiment. This scan test circuit is a circuit for generating a scan test pattern. In figure 12, the same reference numerals as those shown in figure 10 denote the same parts. In figure 12, 80 denotes the replacement circuit and 81 denotes ,against the storage element 28 in figure 10, the replacement circuit which connects the external input signal 12 ,which inputs scan-in data, to the output signal line of the storage element 28. Other constituents are identical to those described for the second embodiment.

[0085]

Since the scan test circuit according to the third embodiment is constructed as described above, the circuit construction becomes the same as that of the conventional scan test circuit shown in figure 18, whereby the above-mentioned scan design protocol is satisfied. Accordingly, when the scan test pattern generated by the scan test circuit of the third embodiment is applied to the second embodiment, the operation

described for the second embodiment can be realized.

[0086]

[Embodiment 4]

In the second embodiment of the present invention, for example, when considering that a first block in the semiconductor integrated circuit executes the scan test described for the second embodiment of the present invention while a second block executes the conventional scan test, there is a problem that passing of desired data from the first block to the second block cannot be satisfactorily carried out during the normal operation.

[0087]

In order to explain this problem, there is provided a scan test circuit shown in figure 13 in which a first block in a semiconductor integrated circuit executes the scan test of the second embodiment of the present invention while a second block executes the conventional scan test. In figure 13, the same reference numerals as those shown in figures 10 and 18 denote the same parts.

[0088]

In figure 13, 158 denotes a combination circuit which receives the output data line 23 of the scan storage element 26, and outputs the normal data line 119. As for other circuit constituents, the first block is identical to figure 10, and the second block is identical to figure 18 except that the normal data line 119 is connected to the combination circuit 158.

[0089]

Figure 14 is a time chart for explaining the operation of the scan test circuit constructed as described above. In figure 14, the same reference numerals as those shown in figure 13 denote the same parts. 700 denote initial data that is stored in the scan storage element 127 in the scan operation, 701 denotes initial data that is stored in the scan storage element 126 in the scan operation, 702~706 denote scan-in data inputted to the external input terminal 112, 708~713 denote normal data on the normal data line 119, 751 denotes data stored in the scan storage element 126 during the normal operation, 720 denotes initial data stored in the scan storage element 27 during the scan operation, 721 denotes initial data that is stored in the scan storage element 26 during the scan operation, 722 denotes initial data that is stored in the scan storage element 25 during the scan operation, 723~727 denote scan-in data of the external input terminal 12, 730 denotes data that is stored in the scan storage element 25 during the normal operation, 736 denotes data that is stored in the scan storage element 27 during the normal operation, and 370 and 371 denote event timings. Other reference numerals denote the waveforms of signals in the signal lines and external terminals corresponding to the reference numerals shown in figure 13.

[0090]

Hereinafter, the operations of the scan test circuit with

the data of normal data line 119, the scan storage element 26, and the scan storage element 125 will be only described with reference to figures 13 and 14. Since the operations of other constituents are identical to those described for the prior art and the second embodiment, it is substituted with the prior arts and the description of the first embodiment.

[0091]

At the event timing 370, the scan storage element 26 ,which is in the scan mode and performs the last-but-one scan operation, continues to hold and output the output data 723 of the scan storage element 25. The combination circuit 158 continues to receive the output data 723 and output the normal data 710 to the normal data line 119. The scan storage element 125 in the normal operation mode holds and outputs the normal data 710 in synchronization with the rising edge of the test clock inputted to the external input terminal 14.

[0092]

At the event timing 371, the scan storage element 67 ,which is in the scan mode and performs the last scan operation, holds and outputs the output data 724 of the scan storage element 25 in synchronization with the rising edge of the normal operation clock at the external input terminal 13. Further, the combination circuit 158 receives the output data 724, and outputs the normal data 11 to the normal data line 119.

[0093]

Originally, the scan storage element 125 must hold and output the output data 711 in the normal operation mode. However, since the last scan operation timing and the normal operation timing of the first block are different from those of the second block, the scan storage element 125 cannot hold and output the output data 711 in the normal operation mode, but holds and outputs the output data 710.

[0094]

So, in this fourth embodiment of the present invention, a required circuit is added between the first and second blocks so that passing of intended data between the blocks becomes possible even when the scan test of the second embodiment of the present invention and the conventional scan test are operated simultaneously, and a stuck-at fault between the blocks can be detected.

[0095]

Figure 15 is a block diagram illustrating the scan test circuit of the fourth embodiment. In figure 15, the same reference numerals as those shown in figure 13 denote the same parts. In figure 15, 150 denotes a fixed data line which is fixed to 1, 152 denotes a controllable scan storage element, 153 denotes an output data line of the scan storage element 152, 154 denotes a monitor storage element, 155 denotes an external output terminal for outputting the output data of the storage element 154, 156 denotes a selector circuit which outputs data of the

output data line when scan selection internal signal of the scan selction internal signal line 16 is "0", and outputs data of the data line 153 when the scan selection internal signal of the scan selection internal signal line is "1" and 157 denotes an output data line of the selector circuit 156. Other circuit constituents are identical to those described with respect to figure 13.

[0096]

Figure 16 is a time chart for explaining the operation of the scan test circuit constructed as described above. In figure 16, the same reference numerals as those shown in figure 14 denote the same parts. Reference numerals 714 and 715 denote normal data on the normal data line 119. Other reference numerals indicate the waveforms of signals at the signal lines and external terminals corresponding to those shown in figures 13 and 15.

[0097]

Hereinafter, the operations of the scan test circuit with the data of the normal data line 119, the scan storage element 26, the scan storage element 125, the scan storage element 152, and the storage element 154 will be only described with reference to figures 15 and 16. Since the operations of other elements are identical to those described for the prior art and the second embodiment, it is substituted with the prior arts and the description of the first embodiment.

[0098]

At the event timing 372, the scan storage element 26 ,which is in the scan mode and performs the last-but-one scan operation, continues to hold and output the output data 723 of the scan storage element 25. On the other hand, since the scan selection internal signal from the scan selection internal signal line 16 is "1", the selector circuit 156 continues to output the output data 724 of the scan storage element 152. The combination circuit 158 receives the output data 724, and continues to output the normal data 711 to the normal data line 119. Further, since the scan selection external signal of the external input terminal 11 transits to "0", the scan storage element 125 is switched to the normal operation mode.

[0099]

At the event timing 373, the scan storage element 125 in the normal operation mode holds and outputs the normal data 711 in synchronization with the rising edge of the test clock of the external input terminal 14. The selector circuit 156 outputs the output data "1" of the controllable scan storage element 152 because the scan selection internal signal of the scan selection internal signal line 16 is "1". The combination circuit 158 receives the output data "1" of the controllable scan storage element 152, and outputs the normal data 714 to the normal data line 119.

[0100]

At the event timing 374, the scan storage element 26 ,which

is in the scan mode and the last operation, holds and outputs the output data 724 of the scan storage element 25. The selector circuit 156 continues to output the output data "1" of the controllable scan storage element 152 because the scan selection internal signal of the scan selection internal signal line 16 is "1". The combination circuit 158 receives the output data "1" of the controllable scan storage element 152, and continues to output the normal data 714 to the normal data line 119.

[0101]

At the event timing 375, the selector circuit 156 outputs the output data 724 of the scan storage element 26 because the scan selection internal signal of the scan selection internal signal line 16 transits to "0". The combination circuit 158 receives the output data 724 of the scan storage element 26, and outputs the normal data 711 to the normal data line 119. However, since no clock enters into the scan storage element 125, the scan storage element 125 does not hold the data 711 from the normal data line 119.

[0102]

At the event timing 376, the monitor storage element 154 holds the output data 724 of the scan storage element 26 and outputs it to the external output terminal 155 in synchronization with the rising edge of the normal operation clock of the external input terminal 13. The selector circuit 156 outputs the output data 735 of the scan storage element 26 because the scan

selection internal signal from the scan selection internal signal line 16 is "0". The combination circuit 158 receives the output data 735 of the scan storage element 26, and outputs the normal data 712 to the normal data line 119. On the other hand, since the scan selection external signal inputted to the external input terminal 11 transits to "1", the scan storage element 125 is switched to the scan mode.

[0103]

As described above, according to the scan test circuit and the scan test control method of the fourth embodiment, the controllable scan storage element, the monitor storage element, and the selector circuit are provided between the first block executing the scan test of the second embodiment of the present invention and the second block executing the conventional scan test, thereby enabling passing of desired data between the first block and the second block. Further, in the normal operation path between the first block and the second block, which comprises the output data line 23, the output data line 157, the combination circuit 158, and the normal data line 119, stuck-at faults in the output data line 157, the combination circuit 158, and the normal data line 119 are detected at the event timing 373, and a stuck-at fault in the output data line 23 is detected at the event timing 376. That is, stuck-at faults between the first block and the second block can also be detected.

[104]

[Embodiment 5]

In the fourth embodiment of the invention, the selector circuit 156 exists in the first path between the scan storage element 152 and the scan storage element 125 and in the second path between the scan storage element 26 and the storage element 154. Therefore, a scan test pattern can be generated for only one of the first path and the second path. So, in this fifth embodiment of the present invention, the selector circuit 156 is replaced with another circuit when generating a scan test pattern, whereby scan test patterns can be generated for both of the first path and the second path.

[0105]

Figure 17 is a block diagram illustrating a replacement circuit that is included in the scan test circuit according to the fifth embodiment, instead of the selector circuit 156 shown in figure 15. In figure 17, the same reference numerals as those shown in figure 15 denote the same parts. In figure 17, 82 denotes a replacement circuit ,instead of the selector circuit 156 in figure 15, which connects the output data line 23 to the output data line 157, and the output data line 153 to the normal data input terminal of the storage element 154.

[0106]

Since the scan test circuit according to the fifth embodiment is constituted as described above, when the scan test pattern that is generated in the scan test circuit of the fifth

embodiment is applied to the fourth embodiment, the scan test operation described for the fourth embodiment is realized.

[0107]

In the embodiments of the present invention, to perform generating the scan selection internal signal of the scan selection internal signal 16 and shifting data in the n-th scan storage element and generating the normal operation clock for performing the normal operation, the normal operation clock of the normal operation clock mask signal 32 is generated in the scan selection internal signal generation circuit having the m-stage (m=1) shift register 45 and the (m+2)-stage shift register 46 as shown in figure 3. However, the generation timing of the normal operation clock mask signal may be changed by constituting an m-stage shift register in which the m is an integer larger than 1 (m>1), thereby changing the generation timing of the scan selection internal signal and the generation timing of the normal operation clock for shifting data in the n-th scan storage element and performing the normal operation.

[0108]

Further, the constructions of the inverter circuit 44, the m-stage shift register 45 (m: integer, m>0), the (m+2)-stage shift register 46, and the EXNOR circuit 49 may be modified as shown in figure 9. That is, in figure 9, the output signals of plural EXNOR circuits are selectable by a selector circuit, whereby plural generation timings of the normal operation clock

can be selected without changing the number of stages of the shift register. As a result, it can arbitrarily select the generation timing of the scan selection internal signal and the generation timing of the normal operation clock for shifting data in the n-th scan storage element and performing the normal operation.

[0109]

Further, in the embodiments of the present invention, the shift-in data, normal operation clock, test clock, and scan selection external signal are supplied from the outside of the semiconductor integrated circuit. However, the shift-in data, normal operation clock, test clock, and scan selection external signal, which are generated in the semiconductor integrated circuit, may be input to the scan control circuit of the present invention.

[0110]

Further, in the fourth embodiment of the present invention, one monitor storage element is prepared for one inter-block normal operation path. However, when plural inter-block normal operation paths are provided, output data lines of plural selector circuits may be bundled using an AND circuit or the like so that data from the data lines are input to a monitor storage element between arbitrary blocks, whereby the number of monitor storage elements can be decreased.

The scan test control method and the scan test circuit

according to the present invention are suitable for detecting a stuck-at fault and a delay fault in a semiconductor integrated circuit.

[111]

[Effects of the invention]

As described above, according to the present invention, in the scan tests control method and the scan test circuit of claims 1 and 8, a scan test circuit incorporating scan chain having n(n: integer, n>0) pieces of scan storage elements, by controlling the frequency of the first clock for shifting in data to the scan storage elements from the external terminal and the frequency of the second clock for shifting in data to n-th scan element and normal operation, both stable input of shift-in data and normal operation can be realized and detection of not only a stuck-at fault but also a delay fault that occur in a semiconductor integrated circuit can be performed effectively.

[112]

Further, according to the present invention, in the scan test circuit of claim 9, by adding storage elements in front of the scan chain having a plural of the scan storage elements, data stored by the scan storage elements during the normal operation becomes identical to the data of the conventional scan test, thereby shift-in data of the conventional scan test can be applied and the same detection ratio of a stuck-at fault that occur in a semiconductor integrated circuit can be maintained.

[0113]

Further, according to the present invention, in the scan test circuit of claim 10, By replacing the scan control circuit and the added storage elements with different circuits respectively, even when there is a scan design protocol that the scan selection external signal supplied from the outside of the semiconductor integrated circuit must be the same as the scan selection internal signal, and the scan-in data supplied from the outside of the semiconductor integrated circuit and the scan-in data inputted to the scan storage elements must be synchronized with each other by a single clock, a scan pattern can be generated without infringing the scan design protocol and detection of not only a stuck-at fault but also a delay fault that occur in a semiconductor integrated circuit can be performed effectively

[0114]

Further, according to the present invention, in the scan test circuit of claim 9, by providing controllable scan storage elements, monitor storage elements and a selector circuit between the first block which carries out the scan test control system described in claim 1 and the second block which carries out the conventional scan test control system, passing of desired data between the first block and the second block becomes possible, whereby, the first block and the second block can be simultaneously subjected to scan test, and a delay fault between

the first block and the second block can also be detected.

[0115]

Further, according to the present invention, in the scan test control method and the scan test circuit of claim 15, by replacing the selector circuit of the scan test circuit in claim 14 with a different circuit, between the first block and the second block, a scan pattern can be generated to the first path between storage elements which synchronize with the first clock and the second path between storage elements which synchronize with the first clock respectively, and constitutions of the scan control method and the scan test circuit of claims 11 to 14 can be realized.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Figure 1]

Figure 1 is a block diagram illustrating a scan test circuit according to a first embodiment of the present invention.

[Figure 2]

Figure 2 is a block diagram illustrating a concrete example of a scan control circuit according to the first embodiment.

[Figure 3]

Figure 3 is a block diagram illustrating a concrete example of a scan selection internal signal generation circuit according to the first embodiment.

[Figure 4]

Figure 4 is a block diagram illustrating a concrete example

of a scan clock generation circuit according to the first embodiment.

[Figure 5]

Figure 5 is a block diagram illustrating a concrete example of an m-stage shift register (m=1) according to the first embodiment.

[Figure 6]

Figure 6 is a block diagram illustrating a concrete example of an m+2-stage shift register (m=1) according to the first embodiment.

[Figure 7]

Figure 7 is a timing chart illustrating the operation of the scan test circuit according to the first embodiment.

[Figure 8]

Figure 8 is a flowchart for explaining a scan test control method according to the first embodiment.

[Figure 9]

Figure 9 is a block diagram illustrating a concrete example of a circuit construction in which the scan selection internal signal generation circuit according to the first embodiment can select plural generation timings of a normal operation clock mask signal.

[Figure 10]

Figure 10 is a block diagram of a scan test circuit according to a second embodiment of the present invention.

[Figure 11]

Figure 11 is a timing chart illustrating the operation of the scan test circuit according to the second embodiment.

[Figure 12]

Figure 12 is a block diagram illustrating the state where a scan control circuit and storage elements in a scan test circuit according to a third embodiment of the present invention are replaced with a replacement circuit.

[Figure 13]

Figure 13 is a block diagram illustrating the scan test circuit indicating the problem of the second embodiment.

[Figure 14]

Figure 14 is a timing chart illustrating the operation of the scan test circuit indicating the problem of the second embodiment.

[Figure 15]

Figure 15 is a block diagram illustrating a scan test circuit according to a fourth embodiment of the present invention.

[Figure 16]

Figure 16 is a timing chart illustrating the operation of the scan test circuit according to the fourth embodiment.

[Figure 17]

Figure 17 is a diagram in which the selector circuit of the scan test circuit according to the fourth embodiment is replaced with another circuit, according to a fifth embodiment of the

present invention.

[Figure 18]

Figure 18 is a block diagram illustrating the conventional scan test circuit.

[Figure 19]

Figure 19 is a block diagram illustrating a concrete example of a scan storage element of the conventional scan test circuit.

[Figure 19]

Figure 20 is a timing chart illustrating the operation of the conventional scan test circuit.

[Description of Reference Numerals]

1...selector circuit

2...scan selection signal input terminal

3...normal data input terminal

4...scan-in input terminal

5...scan clock circuit

6...storage element

11...external output terminal of scan selection signal input terminal

12...external output terminal of scan-in data

13...external output terminal of normal operation clock

14...external output terminal of test clock

15...scan control circuit

16...scan selection internal signal line

17...scan clock signal line

18...combination circuit

19～21...normal data line

22～23...output data line

24...external output terminal which outputs output data of scan storage element 27

25～27...scan storage element

28...storage element

29...output signal line of storage element 28

31...scan selection internal signal generation circuit

32...normal operation clock mask signal line

33...scan clock generation circuit

41...storage element

42...output signal line of storage element 41

43...output signal line of inverter circuit 44

44...inverter circuit

45...m-stage shift register

46...(m+2)-stage shift register

47...output signal line

48...output signal line

49...EXNOR circuit

50...latch circuit

51...storage element

52...output signal line

53...output signal line

54...OR circuit

61...AND circuit

62...output signal line

63...AND circuit

64...output signal line

65...selector circuit

70～73...storage element

80...replacement circuit of scan control circuit 15

81...replacement circuit of storage element 28

82...replacement circuit of selector circuit 156

90～95...storage element

96...inverter

97,98...EXNOR circuit

99...selector circuit

100...external input terminal of selection signal of selector circuit 99

111...external input terminal of scan selection external signal

112...external input terminal of scan-in data

114...external input terminal of test clock

118...combination circuit

119～121...normal data line

122～123...output data line

124...external output terminal which outputs output data of a scan storage element 127

125～127...scan storage element

150...fixed data line

151...external input terminal of scan-in data

152...controllable scan storage element

153...output data line of scan storage element

154...monitor storage element

155...external output terminal which outputs output data of a scan storage element 154

156...selector circuit

157...output data line of selector circuit 156

158...combination circuit

180...initial data which is stored in storage element 28 during scan operation

198...initial data which is stored in scan storage element 27 during scan operation

199...initial data which is stored in scan storage element 26 during scan operation

200～204...scan-in data of external input terminal 12

210～215...normal data of normal data line 19

220～225...normal data of normal data line 20

230～235...normal data of normal data line 21

250～251...normal data of normal data line 19

260～261...normal data of normal data line 20

270～271...normal data of normal data line 21

300～313...event timing

350～355...event timing

360～364...event timing

370～376...event timing

400～403...normal data of normal data line 19

410～413...normal data of normal data line 20

420～423...normal data of normal data line 21

700...initial data which is stored in scan storage element 127 during scan operation

701...initial data which is stored in scan storage element 126 during scan operation

702～706...scan-in data of external input terminal 112

708～715...normal data of normal data line 119

720...initial data which is stored in scan storage element 27 during scan operation

721...initial data which is stored in scan storage element 26 during scan operation

722...initial data which is stored in scan storage element 25 during scan operation

723～727...scan-in data of external input terminal 12

730...data which is stored in scan storage element 25 during normal operation

735...data which is stored in scan storage element 26 during normal operation

736...data which is stored in scan storage element 27 during normal operation

751...data which is stored in scan storage element 126 during normal operation

752...data which is stored in scan storage element 127 during normal operation

800~812...step

1198... initial data which is stored in scan storage element 127 during scan operation

1199... initial data which is stored in scan storage element 126 during scan operation

1200~1204...scan-in data of external input terminal 112

1210~1212...normal data of normal data line 119

1220~1222...normal data of normal data line 120

1230~1232...normal data of normal data line 121

1250~1251...normal data of normal data line 122

1260~1261...normal data of normal data line 123

1270~1271...normal data of normal data line 124

[Name of the Document] Abstract

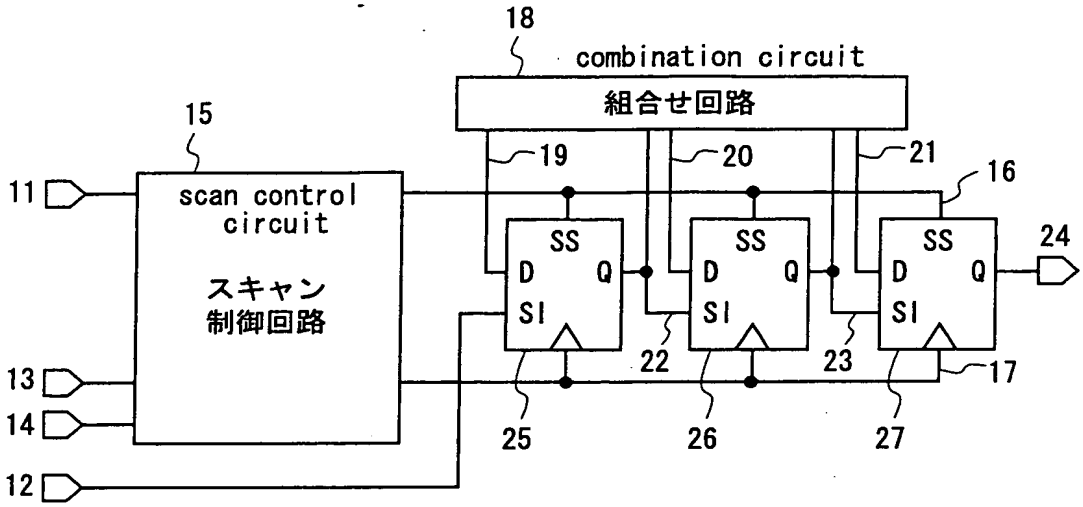
[Summary]

[Object] In the conventional scan test circuit and scan test control method, the scan-in data and the scan selection signal must be directly input to the scan storage elements in the semiconductor integrated circuit from the outside of the semiconductor integrated circuit, as the result, the scan test cannot be carried out as fast as the actual operation speed and a delay fault that relies on a frequency cannot be detected.

[Solution] A scan test circuit is incorporated with a scan chain having a plural pieces of scan storage elements 25, 26 and 27, and provided with a scan clock generation circuit 33 for controlling a frequency of a first clock to be used for shifting data into the first to (n-1)th scan storage elements, and a frequency of a second clock to be used for shifting data into the n-th scan storage element and performing actual operation independently from each other; and a scan selection internal signal generation circuit for generating a scan selection internal signal that is synchronized with the second clock.

[Selected Figure] Figure 1

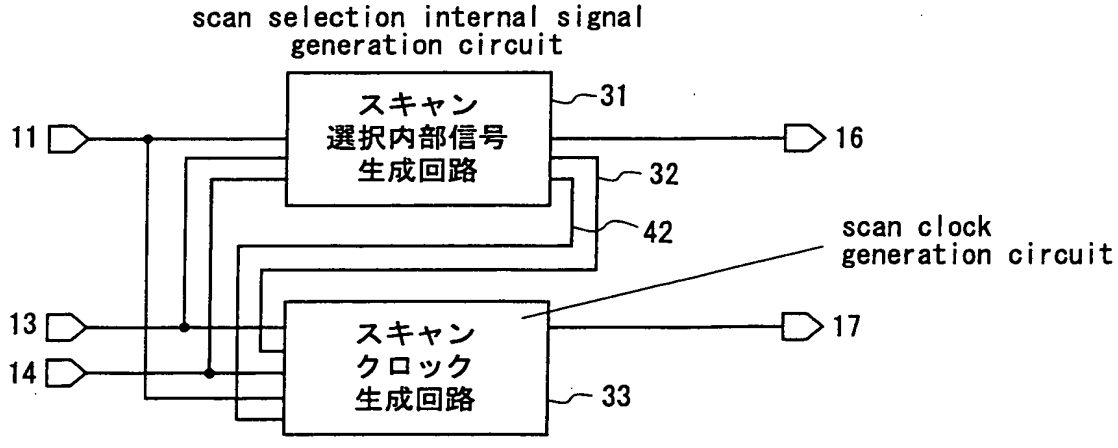
Name of Document
【書類名】 図面 Drawing
【図1】 Figure 1



11：スキャン選択外部信号の外部入力端子
12：スキャンインデータの外部入力端子
13：通常動作クロックの外部入力端子
14：テストクロックの外部入力端子
16：スキャン選択内部信号線
17：スキャンクロック信号線
19～21：通常データ線
22, 23：出力データ線
24：スキャン記憶素子27の出力データを出力する外部出力端子
25～27：スキャン記憶素子

11 : external input terminal of scan selection signal output terimnal
12 : external input terminal of scan-in data
13 : external input terminal of normal operation clock
14 : external input terminal of test clock
16 : scan selection internal signal line
17 : scan clock signal line
19～21 : normal data line
22, 23 : output data line
24 : external output terminal which outputs output data of scan storage element 27
25～27 : scan storage element

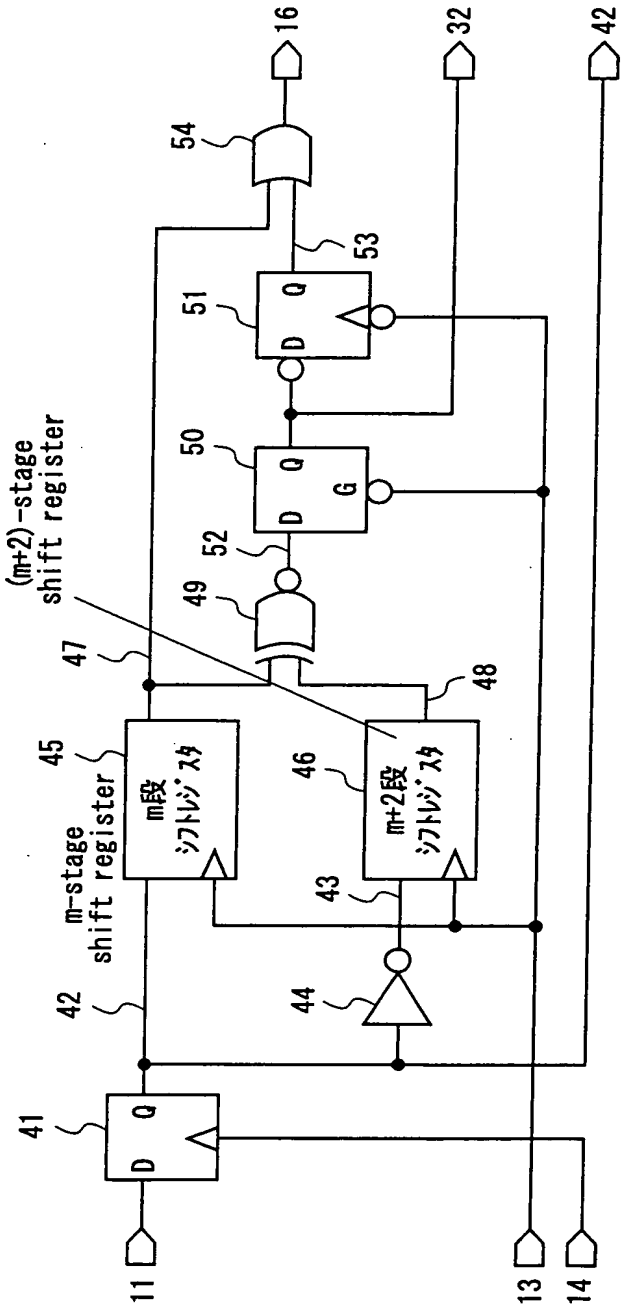
【図2】 Figure 2



32：通常動作クロックマスク信号線
42：記憶素子41の出力信号線

32 : normal operation clock mask signal line
42 : output signal line of storage element 41

【図3】 Figure 3



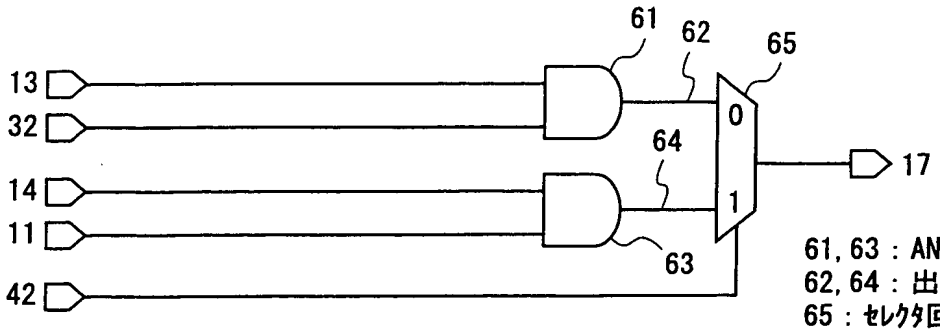
41,51：記憶素子
43：インバータ回路44の出力信号線
44：インバータ回路
47,48,52,53：出力信号線
49：EXNOR回路

50：ラッチ回路
54：OR回路

41,51 : storage element
43 : output signal line of inverter circuit
44 : inverter circuit
47,48,52,53 : output signal line
49 : EXNOR circuit

50 : latch circuit
54 : OR circuit

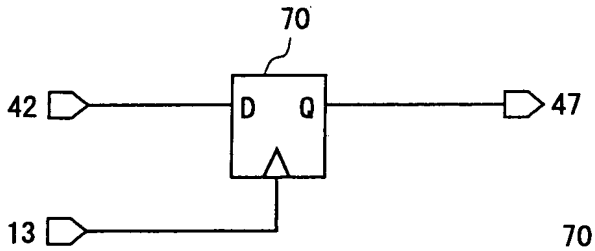
【図4】 Figure 4



61, 63 : AND回路
62, 64 : 出力信号線
65 : ｾﾚｸﾀ回路

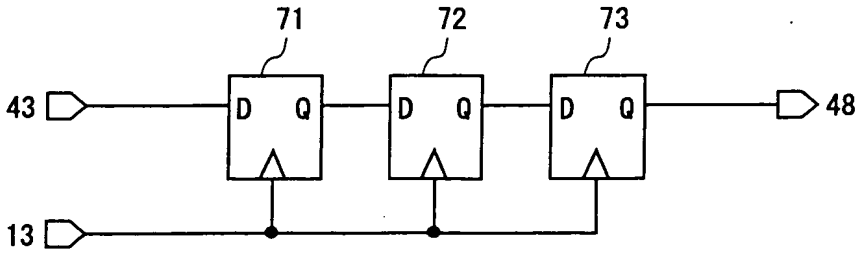
61, 63 : AND circuit
62, 64 : output signal line
65 : selector circuit

【図5】 Figure 5



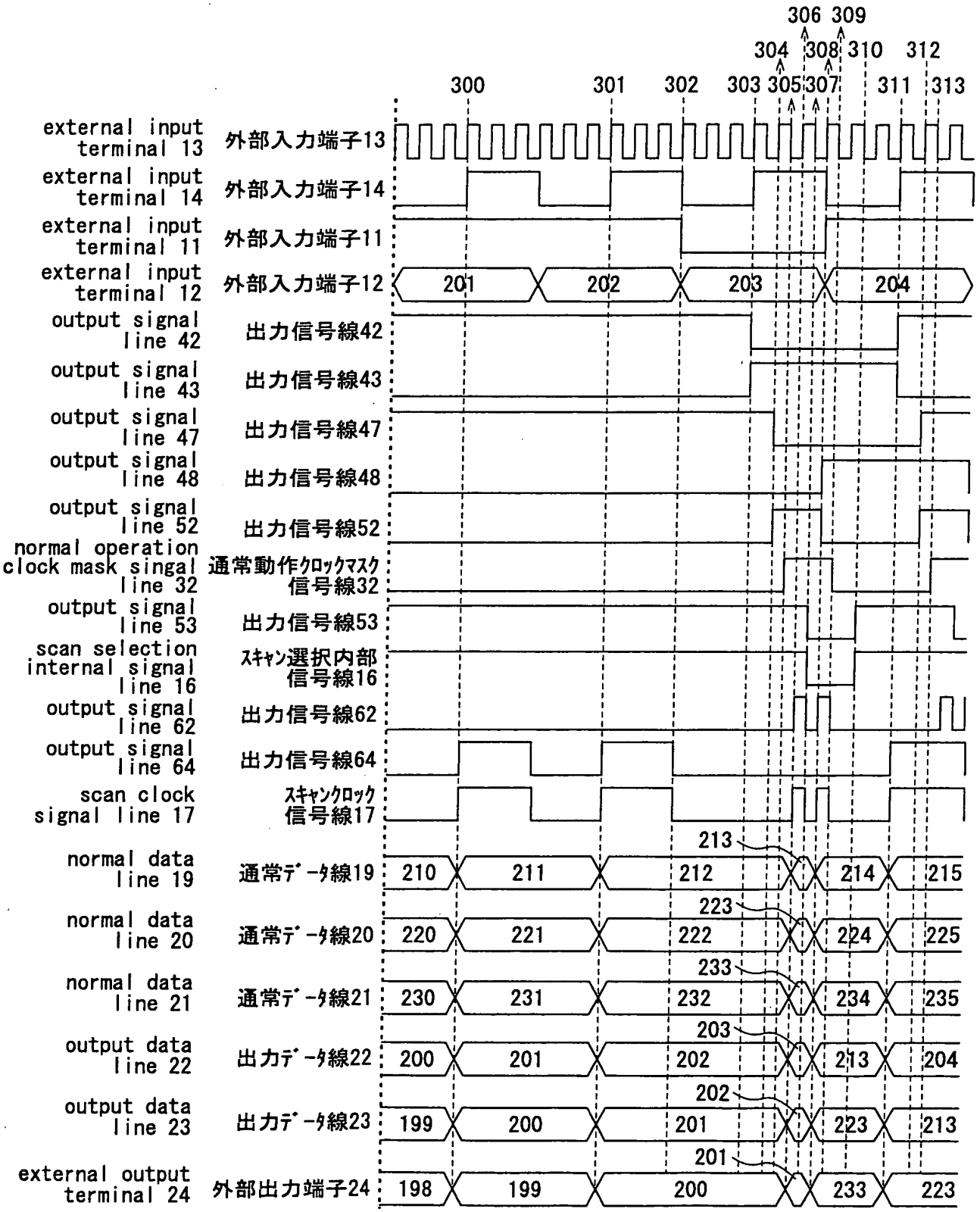
70 : 記憶素子
70 : storage element

【図6】 Figure 5

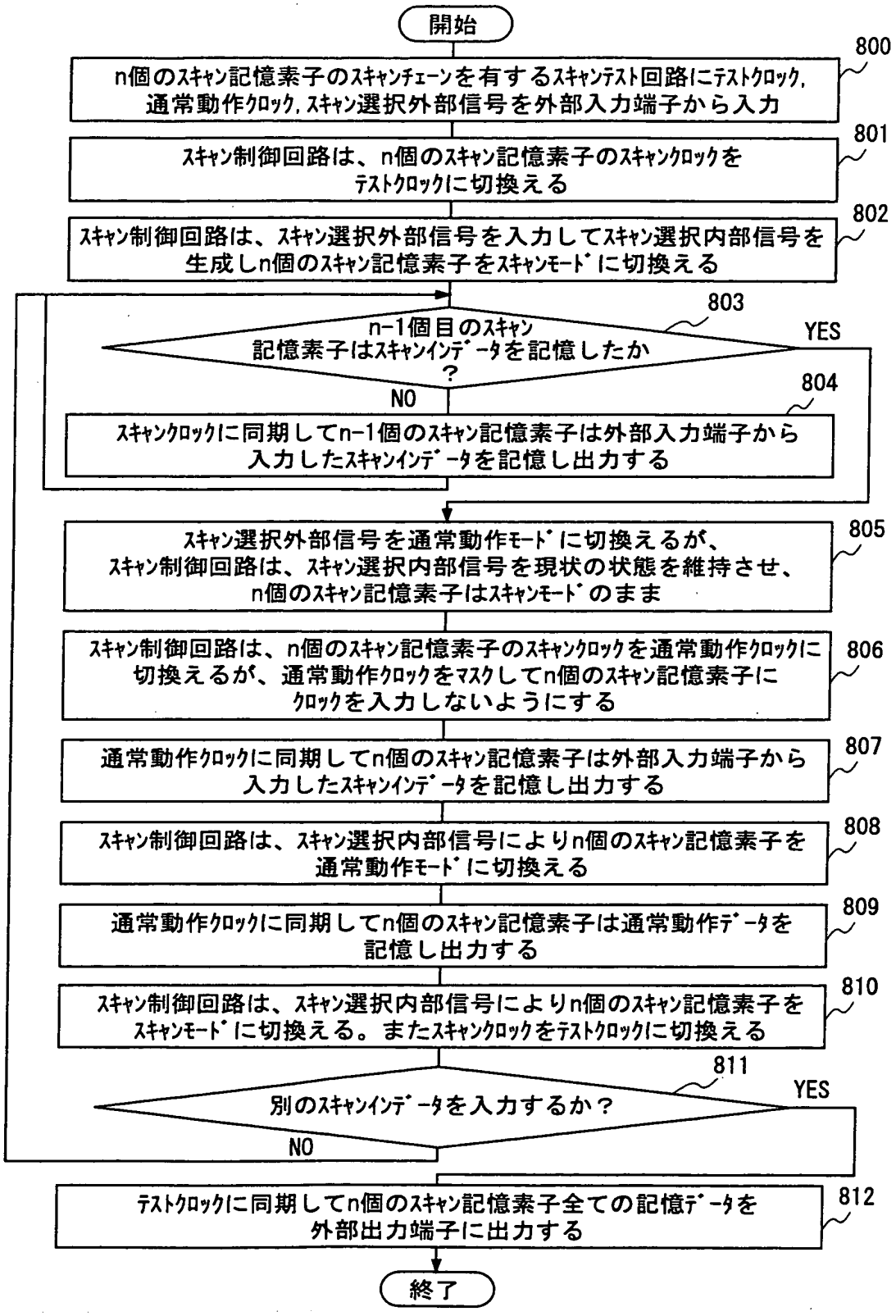


71, 72, 73 : 記憶素子
71, 72, 73 : storage element

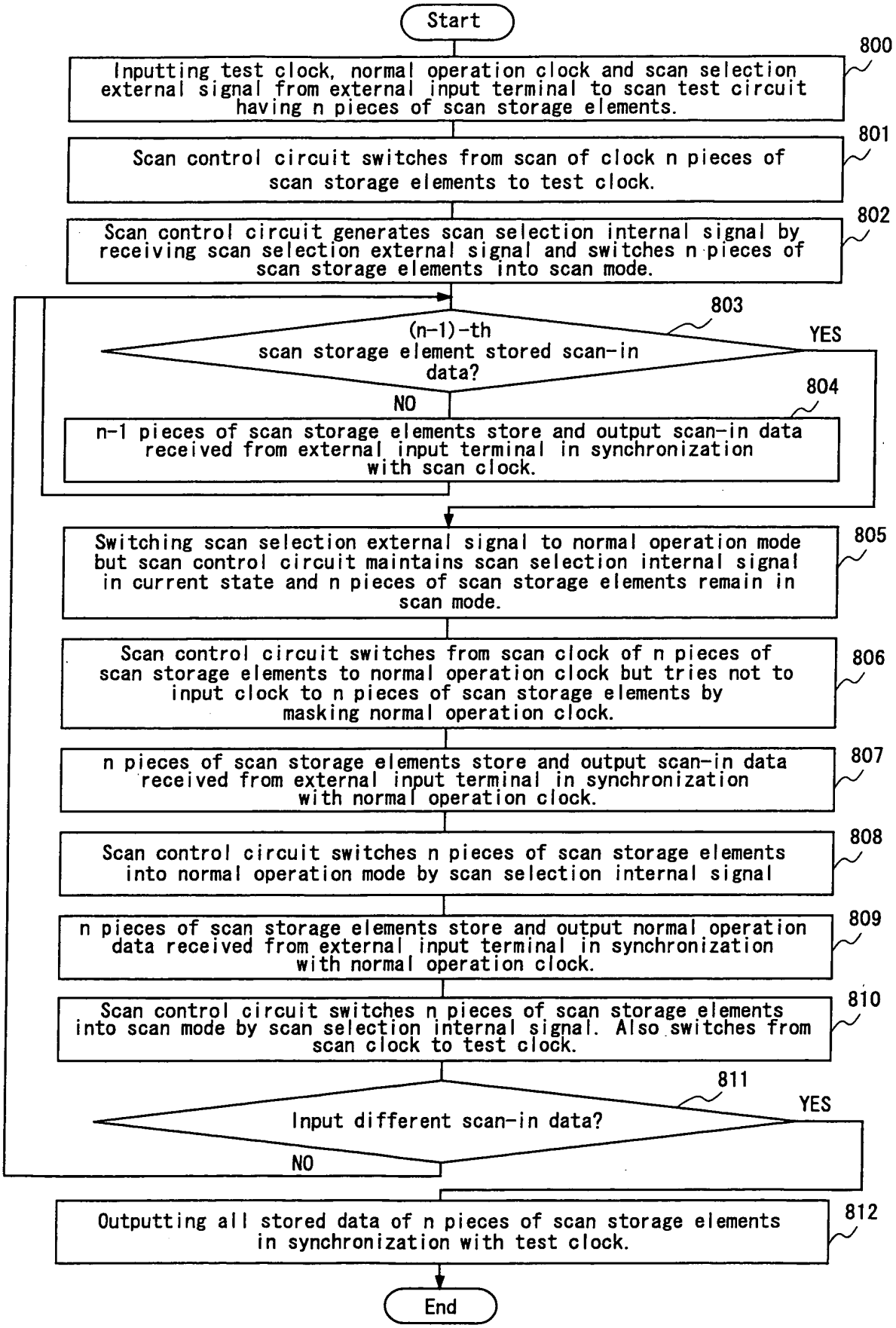
【図7】 Figure 7


306 309
304 308 310 312
300 301 302 303 305 307 311 313
external input terminal 13
外部入力端子13
external input terminal 14
外部入力端子14
external input terminal 11
外部入力端子11
external input terminal 12
外部入力端子12
201 202 203 204
output signal line 42
出力信号線42
output signal line 43
出力信号線43
output signal line 47
出力信号線47
output signal line 48
出力信号線48
output signal line 52
出力信号線52
normal operation clock mask singal line 32
通常動作ｸﾛｯｸﾏｽｸ信号線32
output signal line 53
出力信号線53
scan selection internal signal line 16
ｽｷｬﾝ選択内部信号線16
output signal line 62
出力信号線62
output signal line 64
出力信号線64
scan clock signal line 17
ｽｷｬﾝｸﾛｯｸ信号線17
normal data line 19
通常ﾃﾞｰﾀ線19
210 211 212 213 214 215
normal data line 20
通常ﾃﾞｰﾀ線20
220 221 222 223 224 225
normal data line 21
通常ﾃﾞｰﾀ線21
230 231 232 233 234 235
output data line 22
出力ﾃﾞｰﾀ線22
200 201 202 203 213 204
output data line 23
出力ﾃﾞｰﾀ線23
199 200 201 202 223 213
external output terminal 24
外部出力端子24
198 199 200 201 233 223

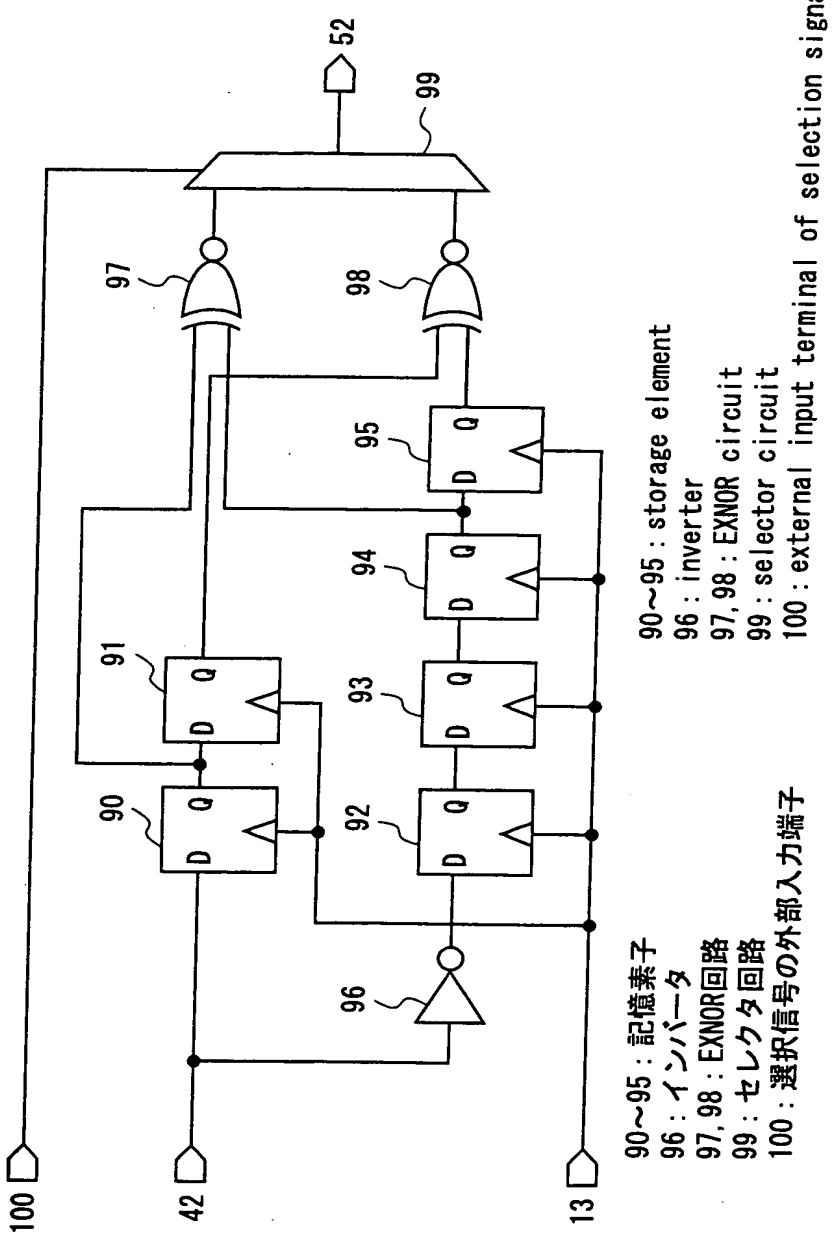
【図8】 Figure 8


開始
800
n個のスキャン記憶素子のスキャンチェーンを有するスキャンテスト回路にテストクロック,
通常動作クロック, スキャン選択外部信号を外部入力端子から入力
801
スキャン制御回路は、n個のスキャン記憶素子のスキャンクロックを
テストクロックに切換える
802
スキャン制御回路は、スキャン選択外部信号を入力してスキャン選択内部信号を
生成しn個のスキャン記憶素子をスキャンモードに切換える
803
n-1個目のスキャン
記憶素子はスキャンインデータを記憶したか
?
YES
NO
804
スキャンクロックに同期してn-1個のスキャン記憶素子は外部入力端子から
入力したスキャンインデータを記憶し出力する
805
スキャン選択外部信号を通常動作モードに切換えるが、
スキャン制御回路は、スキャン選択内部信号を現状の状態を維持させ、
n個のスキャン記憶素子はスキャンモードのまま
806
スキャン制御回路は、n個のスキャン記憶素子のスキャンクロックを通常動作クロックに
切換えるが、通常動作クロックをマスクしてn個のスキャン記憶素子に
クロックを入力しないようにする
807
通常動作クロックに同期してn個のスキャン記憶素子は外部入力端子から
入力したスキャンインデータを記憶し出力する
808
スキャン制御回路は、スキャン選択内部信号によりn個のスキャン記憶素子を
通常動作モードに切換える
809
通常動作クロックに同期してn個のスキャン記憶素子は通常動作データを
記憶し出力する
810
スキャン制御回路は、スキャン選択内部信号によりn個のスキャン記憶素子を
スキャンモードに切換える。またスキャンクロックをテストクロックに切換える
811
別のスキャンインデータを入力するか？
YES
NO
812
テストクロックに同期してn個のスキャン記憶素子全ての記憶データを
外部出力端子に出力する
終了

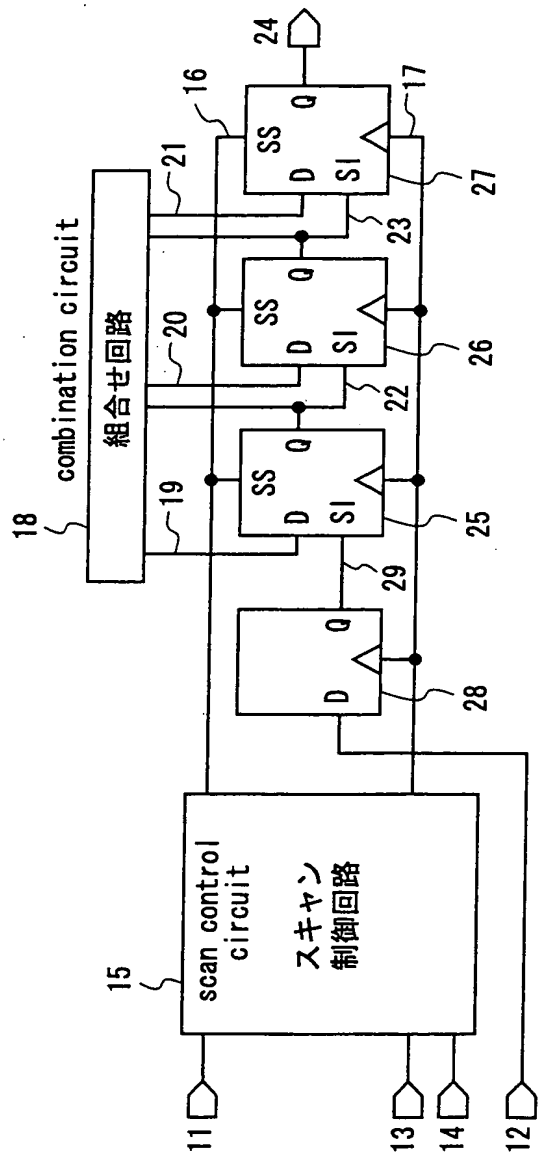
【図8】 Figure 8


Start
800
Inputting test clock, normal operation clock and scan selection external signal from external input terminal to scan test circuit having n pieces of scan storage elements.
801
Scan control circuit switches from scan of clock n pieces of scan storage elements to test clock.
802
Scan control circuit generates scan selection internal signal by receiving scan selection external signal and switches n pieces of scan storage elements into scan mode.
803
(n-1)-th scan storage element stored scan-in data?
YES
NO
804
n-1 pieces of scan storage elements store and output scan-in data received from external input terminal in synchronization with scan clock.
805
Switching scan selection external signal to normal operation mode but scan control circuit maintains scan selection internal signal in current state and n pieces of scan storage elements remain in scan mode.
806
Scan control circuit switches from scan clock of n pieces of scan storage elements to normal operation clock but tries not to input clock to n pieces of scan storage elements by masking normal operation clock.
807
n pieces of scan storage elements store and output scan-in data received from external input terminal in synchronization with normal operation clock.
808
Scan control circuit switches n pieces of scan storage elements into normal operation mode by scan selection internal signal
809
n pieces of scan storage elements store and output normal operation data received from external input terminal in synchronization with normal operation clock.
810
Scan control circuit switches n pieces of scan storage elements into scan mode by scan selection internal signal. Also switches from scan clock to test clock.
811
Input different scan-in data?
YES
NO
812
Outputting all stored data of n pieces of scan storage elements in synchronization with test clock.
End

【図9】 Figure 9


52
99
97
98
95
94
91
93
90
92
96
100
42
13
90～95：記憶素子
96：インバータ
97,98：EXNOR回路
99：セレクタ回路
100：選択信号の外部入力端子
90～95 : storage element
96 : inverter
97,98 : EXNOR circuit
99 : selector circuit
100 : external input terminal of selection signal

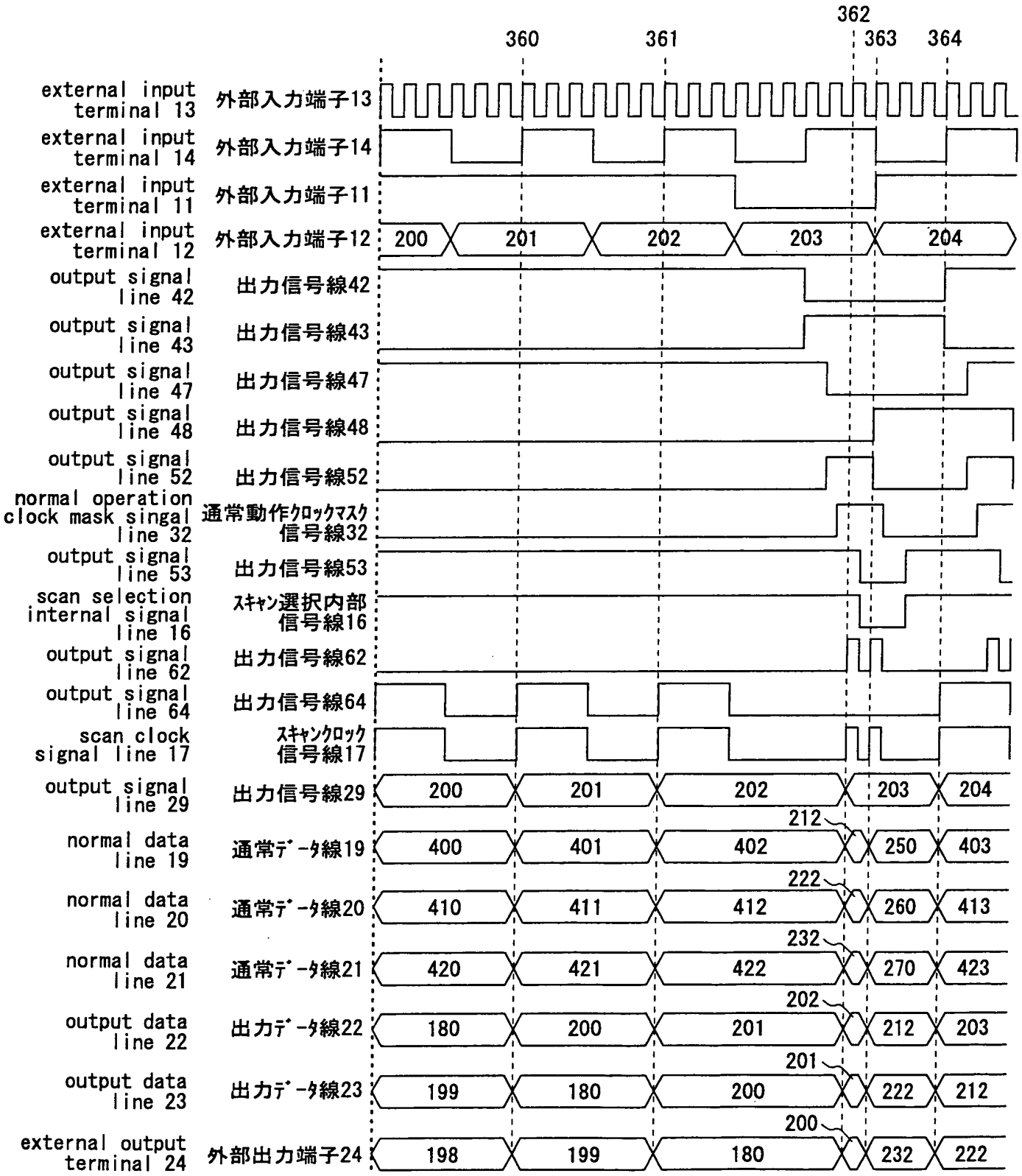
【図10】 Figure 10



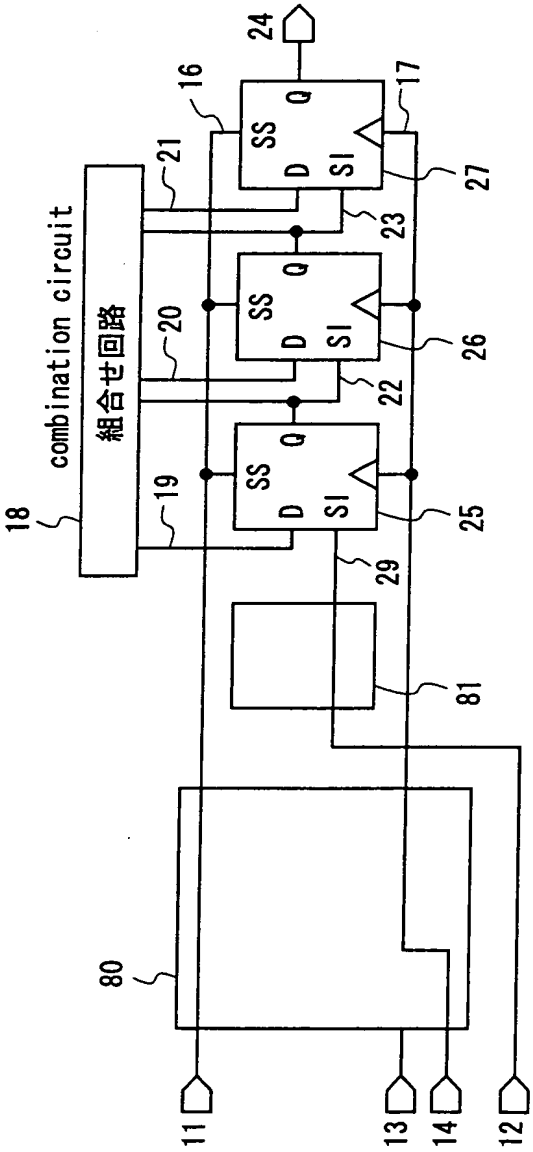
28：記憶素子
29：記憶素子28の出力信号線

28 : storage element
29 : output signal line of storage element 28

【図11】 Figure 11



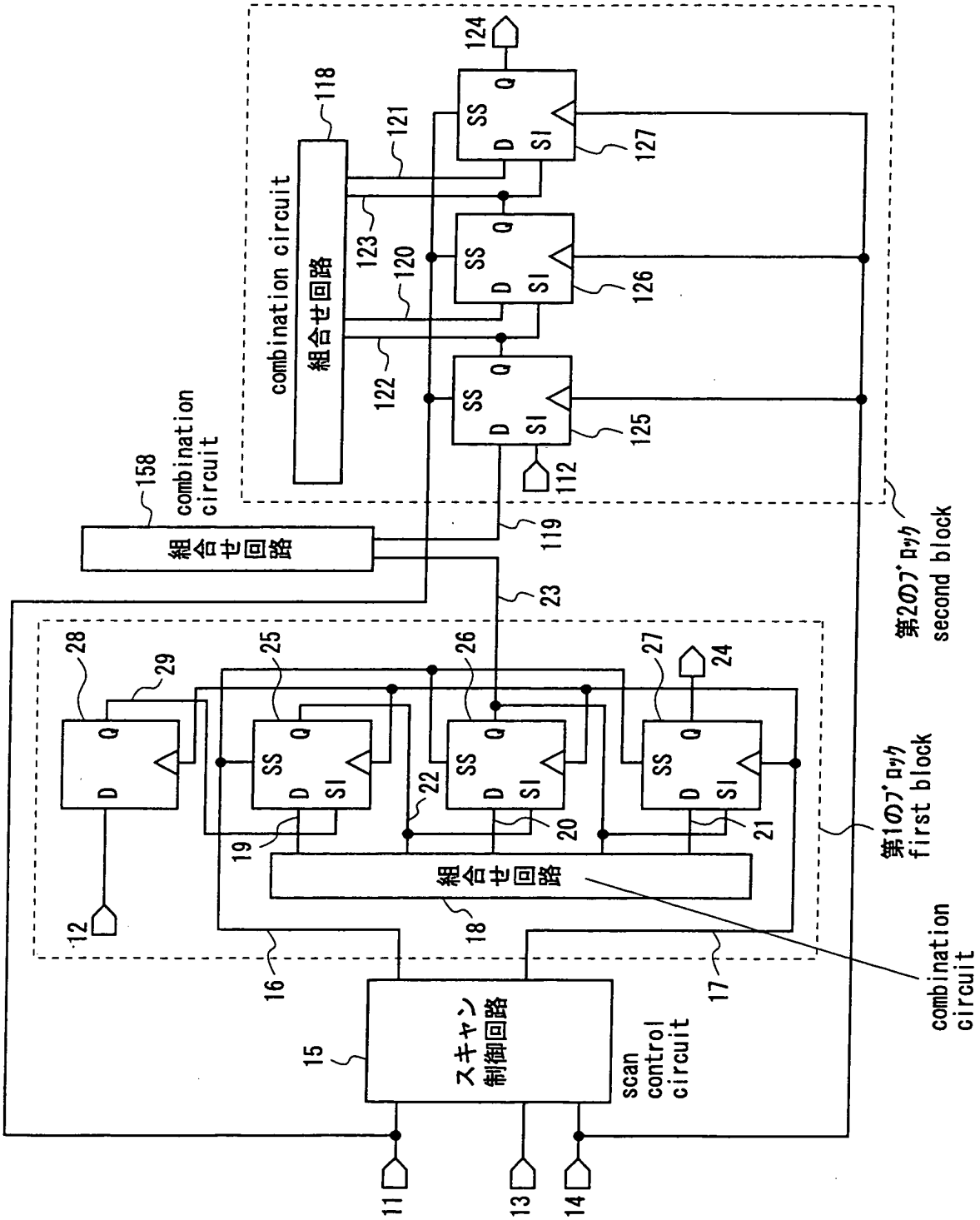
【図12】 Figure 12



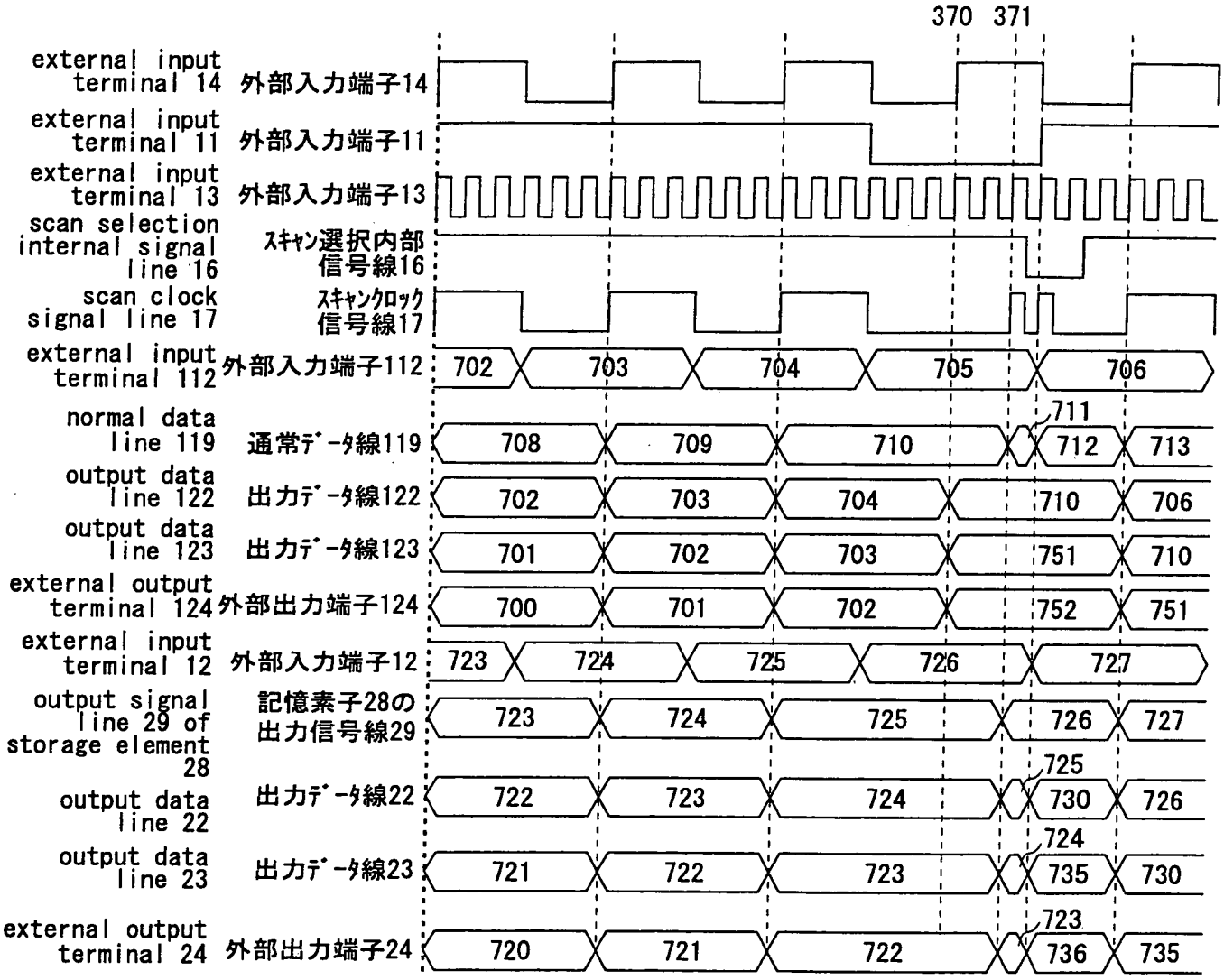
80：スキャン制御回路15の置換え回路
81：記憶素子28の記憶回路

80 : replacement circuit of scan control circuit 15
81 : storage circuit of storage element 28

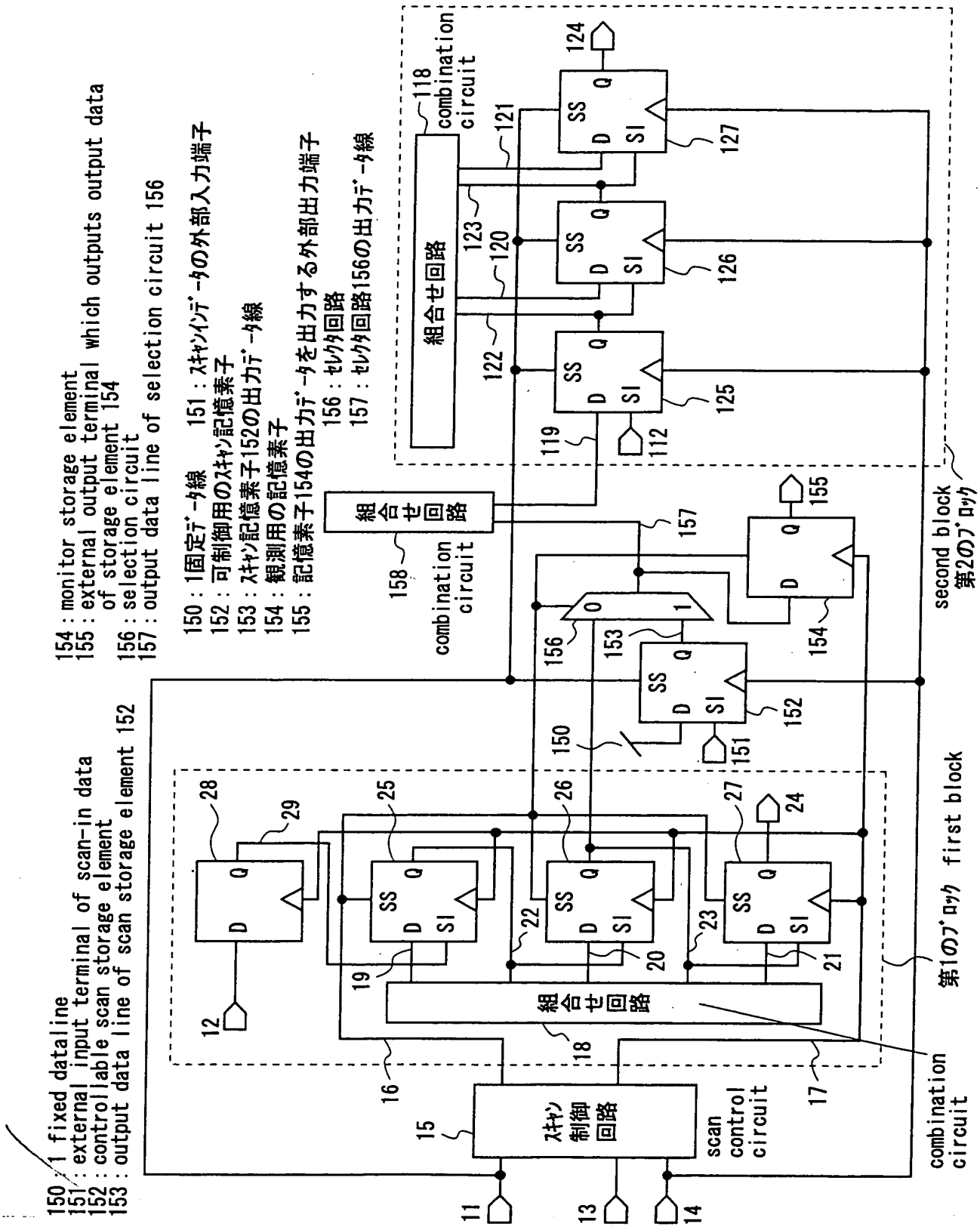
【図13】 Figure 13



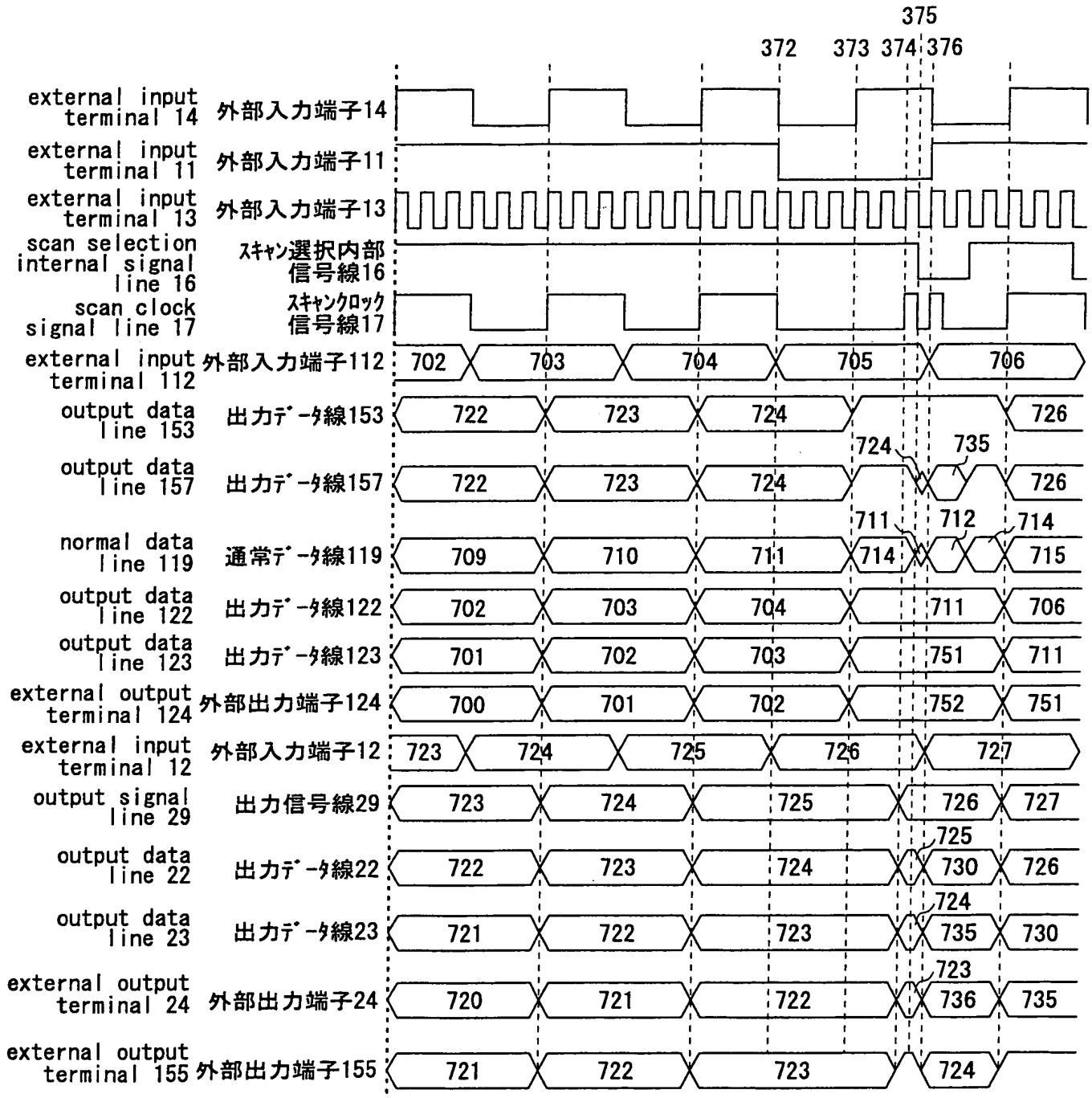
【図14】 Figure 14



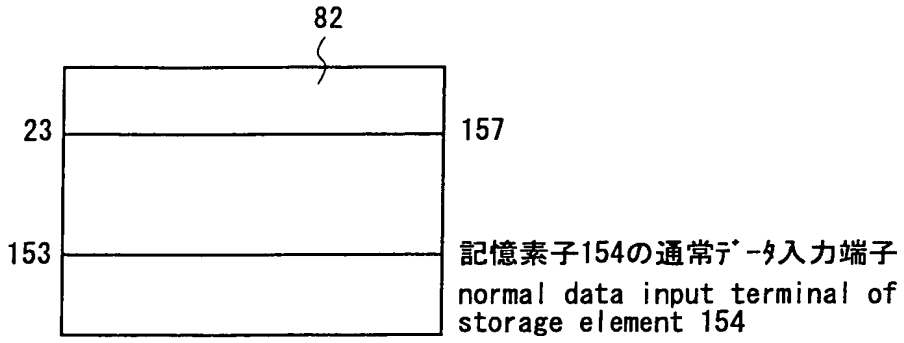
【図15】 Figure 15



【図16】 Figure 16

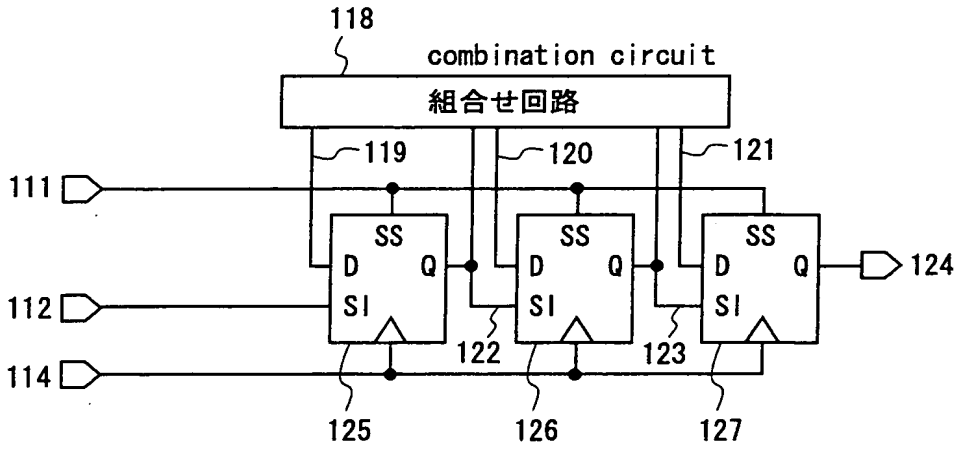


【図17】 Figure 17



82：セレクタ回路156の置換え回路
82 : replacement circuit of selector circuit 156

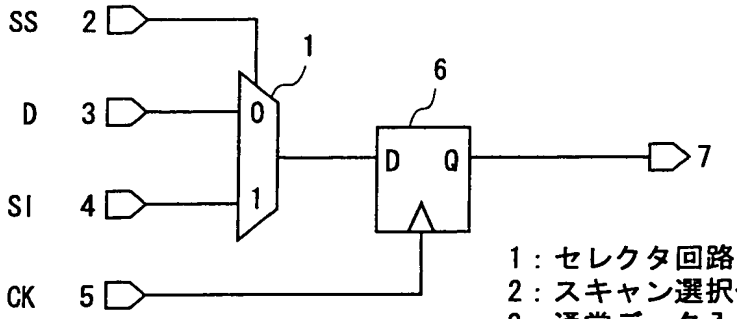
【図18】 Figure 18



111：スキャン選択外部信号の外部入力端子
112：スキャンインデータの外部入力端子
114：テストクロックの外部入力端子
119～121：通常データ線
122, 123：出力データ線
124：スキャン記憶素子127の出力データを出力する外部出力端子
125～127；スキャン記憶素子

111 : external input terminal of scan selection external signal
112 : external input terminal of scan-in data
114 : external input terminal of test clock
119～121 : normal data line
122, 123 : output data line
124 : external output terminal which outputs output data of scan storage element 127
125～127 : scan storage element

【図19】 Figure 19



1：セレクタ回路
2：スキャン選択信号入力端子
3：通常データ入力端子
4：スキャンイン入力端子
5：スキャンクロック入力端子
6：記憶素子
7：出力端子

1 : selector circuit
2 : scan selector signal input terminal
3 : normal data input terminal
4 : scan-in input terminal
5 : scan clock input terminal
6 : storage element
7 : output terminal

【図20】 Figure 20